TECHNISCHE UNIVERSITÄT
CHEMNITZ

Aufgabenstellung

zur

Abschlussarbeit
im Studiengang Master Micro and Nano Systems

für

Herrn Joydeep Ghosh
geb. am 16. September 1982 in Kolkata

zum Thema

Fabrication of laterally stacked spin devices by semiconductor processing

(ausführliche Aufgabenstellung siehe Rückseite)

Betreuender Hochschullehrer: Prof. Dr. Thomas Geßner
Ausgabedatum: 01.09.2010
Abgabedatum: 09.02.2011
Tag der Abgabe:

Unterschrift: .....
Prof. Dr. J. T. Horstmann
Vorsitzender des Prüfungsausschusses

Table of Contents: Pages

Abbreviations and acronyms:

Terminology:

MEMS	Micro Electro Mechanical Systems
RF	Radio Frequency
HARMS	High Aspect Ratio Microstructure Systems
RIE	Reactive Ion Etching
DRIE	Deep Reactive Ion Etching
BDRIE	Bonded and Deep Reactive Ion Etching
SOI	Silicon on Insulator
SOG	Silicon on Glass
AIM	Air gap Insulated Microstructure
SCREAM	Single Crystal Reactive ion Etching and Metallization
GMR	Giant Magnetic Resistance
TMR	Tunneling Magnetic Resistance
TAMR	Tunneling Anisotropic Magnetic Resistance
AMR	Anisotropic Magnetic Resistance
CMR	Colossal Magnetic Resistance
SP	Spin Polarization
DOS	Density Of States
JDOS	Joint Density Of States
IC	Integrated Circuit
CVD	Chemical Vapour Deposition
APCVD	Atmospheric Pressure CVD
SACVD	Sub Atomic pressure CVD
LPCVD	Low Pressure CVD
UHVCVD	Ultra High Vacuum CVD
PECVD	Plasma Enhanced CVD
TO	Thermal Oxidation
ALD	Atomic Layer CVD
MOCVD	Metal Organic CVD
ICP	Inductively Coupled Plasma
CCP	Capacitively Coupled Plasma
ICP-RIE	ICP used in RIE
ICPE	Inductively Coupled Plasma Etching
VCSEL	Vertical Cavity Surface Emitting Lasers
AR	Aspect Ratio
NA	Numerical Aperture
DOF	Depth of Focus
FIB	Focused Ion Beam
LEED	Low Energy Electron Diffraction
RAM	Random Access Memory
MRAM	Magnetoresistive RAM
DRAM	Dynamic Random Acess Memory
SRAM	Static Random Acess Memory
FET	Field Effect Transistor
LED	Light Emitting Diode
OLED	Organic LED

TFT	Thin Film Transistor
LCD	Liquid Crystal Display
SEM	Scanning Electron Microscope
XRD	X-ray diffraction
AFM	Atomic Force Microscopy
STM	Scanning Tunneling Microscopy
SE	Secondary Electrons
BSE	Back Scattered Electrons
CRT	Cathode Ray Tube
FM	Frank-van der Merwe growth
VW	Volner Weber growth
SK	Stranski Krastanov growth
OMBD	Organic Molecular Beam Deposition
RT	Room Temperature
TF	Test Field
ZfM	Zentrum für Mikrotechnologie
ENAS	Einrichtung für elektronische Nanosysteme
IBM	International Business Machine
RAMAC	Random Access Method of Accounting and Control
MFM	Modified Frequency Modulation
RLL	Run Length Limited
PRML	Partial Response Maximum Likelihood
AC	Alternating Current
DC	Direct Current
GHz	Giga Herz
UV	Ultra Violet
sccm	standard cubic centimeters per minute
slm	standard liters per minute
mTorr	mili Torr
Pa	Pascal, 1 Torr = 133,32 Pa

Chemistry:

Si	Silicon
O_2	Oxygen
SiO_2	Silicon-di-oxide
Co	Cobalt
Fe	Iron
Cr	Chromium
Co	Cobalt
Cu	Copper
Au	Gold
Pt	Platinum
Ar	Argon
FePc	Iron Phthalocyanine
CuPc	Copper Phthalocyanine
MnPc	Manganese Phthalocyanine

TEOS	Tetraethyl Orthosilicate, $Si(OC_2H_5)_4$, 4 ethyl groups attached to SiO_4^{4-}
Fe_3O_4	Magnetite
$MgFe_2O_4$	Magnesioferrite
CF_4	Carbon tetrafluoride
SF_6	Sulfur hexafluoride
NF_3	Nitrogen trifluoride
Cl_2	Chlorine gas
KOH	Potassium hydroxide
HF	Hydrogen fluoride or hydrofluoric acid
H_3PO_4	Phosphoric acid
C_4F_8	Octafluorocyclobutane
S_xF_y	Sulfur fluorine complex
Alq_3	8-hydroxyquinolinato aluminium, Al $(C_9H_6NO)_3$
Ga	Gallium

Other symbols:

N_{ox}	SiO_2 molecular density, 2,3. 10^{22} molecules/cm^3
N_{Si}	Atomic density of Silicon, 5. 10^{22} molecules/cm^3
eV	electron Volt
KeV	Kilo electron Volt
E	Energy
G	Gibb's free energy
γ	Surface energy
E_f	Fermi level energy
E_g	Band gap energy
ρ	Specific resistivity
σ	Conductivity
λ	Wavelength
χ	Magnetic susceptibility
μ_0	Magnetic permeability (of vacuum)
μ_r	Magnetic permeability (relative)
K	Boltzmann constant, 1.3806503×10^{-23} m^2 kg s^{-2} K^{-1}
c	Light velocity, 300,000 kilometers/sec

1. Introduction

1.1 Abstract:

This work represents a new attempt of fabricating devices to realize spin transport through trench and/or on the surface via a transport channel. The science regarding electron spin, spin degree of freedom along with electronic charge, spin transport, magneto resistance has been a huge research topic over a decade, especially in the field of data storage and magnetic sensors. It is believed that extending conventional electronics to spin-electronics can yield devices with new functionality and result in new large scale applications. Here, the main emphasis is on spin transport at room temperature in the trench between two metallic ferromagnets. Spin transport can happen in a vertical channel, horizontal channel, inside a trench or any other Geometry. The transport medium used is organic semiconductors. The electronic transport in some hundred nanometers of organic molecular channel is a subject of immense interest, and to monitor transport phenomena properly, one needs to have very short and properly designed trenches. The molecular transport channel was prepared by different technological steps (lithography, deep reactive ion etching, oxide deposition, metal sputtering and organic molecular beam deposition) and design considerations.

1.2 Motivation:

This thesis was performed with couples of goals in mind. First is to understand and have better ideas about nanotechonolgy, different processes and measurement techniques. A great deal of focus is on different deposition techniques, their comparative studies and so on. It is exciting to develop a desired nanostructure by a series of processes, and one needs to define the process steps very carefully. The other goal was to study on molecular spintronics and its applicability. It was really challenging to reach a dimension of even less than 100 nm, depositing molecular crystals in it, check for the proper structures whether and how the molecules fill up the trenches and then go for an experiment for spin transport in such a small trenches. It was exciting to try to find how organic molecules behave (electrically and magnetically) in small trenches. There were no certain guidelines available to reach the goal and hence this topic demands a great deal of understanding about the microtechnology, physics and other important fields of science. More knowledge and more understanding would be developed once one works on this topic.

1.3 MEMS Technology:

A short overview of MEMS technology is discussed, the project uses SCREAM structure which is frequently used in MEMS domain. MEMS technology involves a combination of micro sensors and micro actuators and electronic devices integrated on a single chip. In a MEMS device, all the electrostatic, fluid mechanical, thermo mechanical and electro mechanical components are present. In fact, the definition and application of any microsystem differs from researcher to researcher. Current microsystems operate within several energy domains like, mechanical (including mechanical state like position, velocity, acceleration, stress, strain, deformation, mass etc), electrical (voltage, electric field, current, impedance, frequency, phase etc), thermal (temperature, conductivity, thermal impedance), magnetic (magnetic field, moment, permeability and susceptibility), chemical (potential, concentration, reaction rate), radiation (intensity, wavelength, phase, polarization) etc.[8]

1.3.1 Use:

MEMS devices can be used like any kind of inertial sensor, RF and Optical switches. Inertial sensors include rate sensing elements (e.g. accelerometer, gyroscopes) or pressure sensors. They find application in optical spectroscopy field like MEMS spectrometer, IR micro spectrometer. MEMS find usage in mobile communication domain too (RF MEMS).

1.3.2 MEMS Fabrication:

MEMS manufacturing can be of two types, surface micromachining and bulk micromachining. In surface micromachining, structures are built on the top of the substrate, and the technology involves deposition (on the wafer top) and etching of different layers to form a certain geometry. The property of the substrate is not that important and hence expensive silicon wafers can be replaced by glass etc. Bulk micromachining involves selective etching inside the substrate (unlike surface micromachining which produce the structure on the top).
The bulk micromachining includes HARMS technology which might encompass more sophisticated technologies like BDRIE, SOI or SOG, AIM, SCREAM. SCREAM is also a type of HARMS technology, where high aspect ratio silicon microstructures are produced with metalized sidewalls. The bulk silicon can be used both as the structural and sacrificial layer. SCREAM is a low cost process and simple. Bulk technology may also involve different wafer bonding technologies like direct bonding, anodic bonding, eutectic bonding or adhesive bonding etc [1] [4].

1.3.3 MEMS SCREAM structure:

The use of monocrystalline silicon to produce MEMS has several advantages like [5] [3],

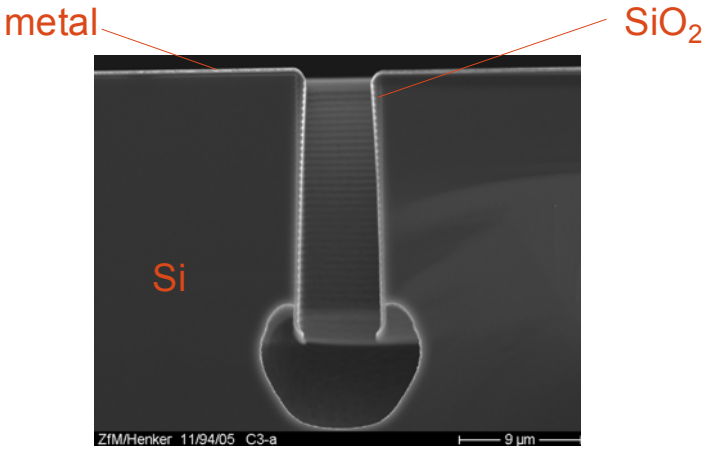


Figure 1.1: Typical SCREAM structure

- Good mechanical properties compared to polycrystalline silicon.
- In semiconductor device fabrication, monocrystalline form is used because they lack impurities and crystallographic defects, which, in turn, affects material electronic properties. So, co-integration of mechanical properties with associated electronics produces good result.

In this project, as main focus is on device fabrication for molecular spin transport study (near the surface, inside the trenches and within two metallic electrodes), SCREAM is chosen.

1.4 Organic electronics:

This part of electronics deals with organic molecules instead of only inorganic molecules like Silicon and other stuffs. Now a days, this branch of electronics has a lot of application areas like in Sensors, OLEDs (Alq3 8-hydroxyquinolinato Aluminium complex is used along with other polymers), organic lasers, solar cells (phthalocyanine complex are used), organic TFTs, rechargeable batteries, display systems and much more. Organic photoconductors were invented in 1970's and OLED was published in 1987. Much focus was on organic transistors from these times with a realization of organic transistors. Polymer LEDs were developed and afterwards the conductive polymers were discovered. Organic electronics consists of low temperature processes making itself low cost system. These materials are well compatible with inorganic materials. A major drawback of organic electronics has been lower carrier mobility (e.g. inorganic material shows a carrier mobility of 1 to 1500 whereas organic material shows below 0,001, units are in Cm^2-V/sec). Research is going on to improve their stability as well [36].

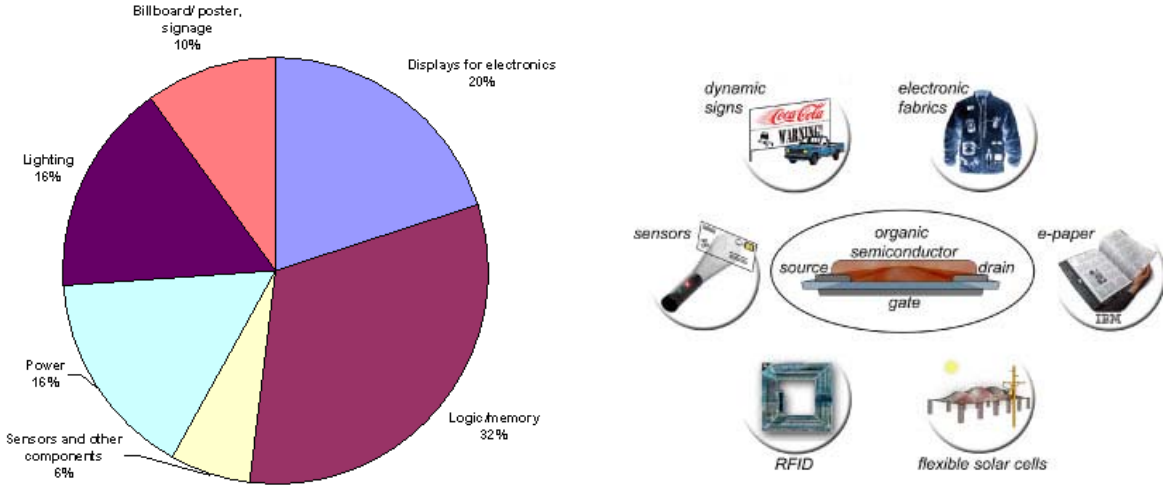


Figure 1.2: Images showing Organic electronics market, applicability and usage in modern world

1.5 Molecular Spintronics:

The concept of molecular magnetism and electron spin transport is discussed. Historical backgrounds are important for an insight towards development of this scientific field.

1.5.1 History of magnetic storage and spintronics:

Electron was invented way back in 1897 by J. J. Thomson, who was working on Cathode rays. Electron charge was then measured to perfection (Oil drop experiment, R. Millikan). The presence of magnetic moment of electron was discovered in the year of 1922 (‘Stern’ and ‘Gerlach’) and later it was also established that electron spin is quantized (spin ‘up’ or spin

‘down’). The first observation of spin affecting electron transport dates back to 1857, when W. Thomson found that the resistivity of bulk ferromagnetic metals depended on the relative angle between the electric current and the magnetization direction (i.e. AMR). A study on spin polarized tunneling on ferromagnetic/insulator/superconducting aluminum junctions was made by ‘Tedrow’ and ‘Meservey’. In 1975, ‘Julliere’ invented an increase in resistance (~10 % at low temperature, 4,2 K) when the magnetic layers in Fe/Ge/Co switched from the parallel to the anti parallel configuration (the first experiment on TMR, much stronger than AMR effect). Much concentration is put on this topic from then after and people observed maximum around 20 % of TMR at room temperature [20].
From 1980's, scientists became able to fabricate multilayered devices with each layer thickness in the range of nanometers. In 1986, Brillouin scattering experiments of Peter Grünberg and coworkers revealed the existence of antiferromagnetic interlayer exchange couplings in Fe/Cr multilayers. Fe/Cr appeared as a magnetic multilayered system in which it was possible to switch the relative orientation of the magnetization in adjacent magnetic layers from anti parallel to parallel by applying a magnetic field. GMR was discovered in 1988 independently by ‘Albert Fert’ (French scientist) and ‘Peter Gruenberg’ (German scientist). Since then, this has become a research field to look for. They were awarded Nobel Prize in Physics (2007) for this contribution. IBM took step to work about GMR on thin film structures. They introduce the first GMR hard disc head. Physicists from the University of Arkansas successfully injects a stream of electrons with identical spins into a semiconductor in 2001. In the year of 2003, a successful way of transferring electron spin across molecular bridge between quantum dots is achieved. First organic 'spin valve' comes to existence in 2004, and new Spintronic Speed Record - 2 GHz MRAM devise comes into realization in 2005. In the same year, the Petabyte data storage was possible. Spin Hall effect is detected at room temperature in the year of 2006. Scientists discover magnetic super atoms in 2009, spin field effect transistors come to realization in this year as well. Researchers were able to detect and manipulate spin at room temperature those days. Research has also been done to generate spin current in Graphene structure and are able to read the spin of a single electron these days. The spintronics science has evolved in a fast way and there are still a lot of things to study for.

A brief note on magnetic storage devices is also mentioned. In fact before presence of any kind of magnetic storage systems for computers, people used punch cards (or Herman Hollerith card) as primary storage medium. A group of IBM engineers began working on magnetic storage sciences in 1949. On May 21, 1952, IBM announced the IBM 726 Tape Unit with the IBM701 Defense Calculator, marking the transition from punched-card calculators to electronic computers. On September 1956, a small team of IBM engineers introduced the first computer disk storage system as part of the 305 RAMAC computer. The device could store 5 million characters (only 5 MB) of data on 50 disks. The storage device becomes faster. From these beginnings, the magnetic storage industry has progressed such that today one can store 500 GB or more on tiny 3,5 inch drives that fit into a single computer drive bay. IBM research has been pioneer for magnetic storage sciences, be it hard drive or floppy drive. IBM has also pioneered advanced magnetic data encoding schemes, such as MFM and RLL; drive head designs, such as thin film, magneto-resistive, and GMR heads; and drive technologies, such as PRML, No-ID recording, and Self-Monitoring Analysis and Reporting Technology.

Today's conventional electronics does not use the spin of the electrons and relies only on the transport of the electron charge. Physicists are now trying to exploit the electron spin in order to create novel devices with a broader functionality. This gives rise to rapidly developing science of Spintronics. Spintronics has the future of increasing data storage capacity, increased data processing speed, decreased electric power consumption. Technology can

either use only electron spin or both spin with charge into consideration to build the devices, this gives an extra degree of freedom. This part of science also needs a development in new materials. In reality, one has seen a growth of spintronics in last 20 years and it is used in hard disc technology with a promising future application to get into RAM of today's computers. The concept of Spin FETs based on spin transport in semiconductor lateral channels between spin-polarized source and drain with control of the spin transmission by a field effect gate can also be realized in near future. Among other research fields, scientists look for the fabrication of ferromagnetic semiconductors and thus enhancing the possibility of controlling the ferromagnetic properties with a gate voltage. A practical situation will arise when scientists can discover room temperature ferromagnetic semiconducting devices. Another research field is dealing with spin polarized currents induced by spin-orbit effects (spin-orbit interactions deflect the currents of the spin 'up' and spin 'down' channels in opposite transverse directions, thus inducing a transverse spin current, even in a nonmagnetic conductor, which could be used to create spin currents in structures composed of only nonmagnetic conductors). [19 - 26]

1.5.2 Theory behind:

Nanotechnology deals with nanostructures, whose at least one dimension is in nanometer range. Nanostructures can be of 0 dimensional (nanoparticles) or 1 dimensional (nanowires and rods) or 2 dimensional (thin films) or even 3 dimensional. The term 'Nanotechnology' may describe a lot of scientific areas like MEMS, bottom up technology (e.g. self assembly), thin film growth and characterization or even drug delivery inside a carbon nanotube. Measurement techniques in nanoscience also play vital role in nanostructure characterization as this demands sensitivity, accuracy, and atomic level resolution. The tools used to characterize these nanostructures are SPM, SEM, TEM etc and SEM is one of the most widely used techniques to characterize nanostructures these days. For specifically surface analysis, one uses AFM, STM etc. For crystal characterization and chemical analysis, one can use XRD, EDX. It is vital to measure the film thickness, film profile, electrical properties (like resistance, capacitance, resistivity, sheet resistance, permittivity etc.), optical and magnetic properties and so on. For this, different types of profilometers (contact or non-contact type) and other instruments are used. For film resistance measurement, two probe or four probe technique could be used [9] [17]. In this project, some of these technologies are used and discussed in corresponding sections.
All the important phenomena regarding spintronics science are discussed in brief.

1.5.2.1 Electron spin:

Electron spin was discovered in 1925, spin is one of the fundamental features of electron along with its other basic properties like mass and charge. Electron spin is related to its intrinsic angular momentum as angular momentum is characterized by self electron rotation about its own axis. These concepts gave rise to fourth quantum number of the elementary particles. The spin angular momentum is characterized by a quantum number, $s = 1/2$ for electrons. Spintronics science takes care of electron spin (along with electronic charge) and corresponding magnetic moment for fabrication of new devices [33].

1.5.2.2 Solid state magnetism:

To have a better understanding to this project, one needs to have knowledge on molecular magnetism. The description of magnetism in a solid body is dependent on electrons (atomic nucleus also shows the same properties but they are much lower compared to electrons),

whether they are localized (on ion cores) or delocalized (forming bands). Electrons are the prime source of magnetic moments in solids. Electron is the elementary particle and has a mass 'm_e' and charge (-e). From basic principles, it is known that any charged body under circular motion will exhibit magnetic moment depending on the direction of rotation. Electrons, though, have two distinct sources of angular momentum,

(a) Due to orbital motion i.e. rotation around the nucleus.
(b) Due to electron spin around its own axis.

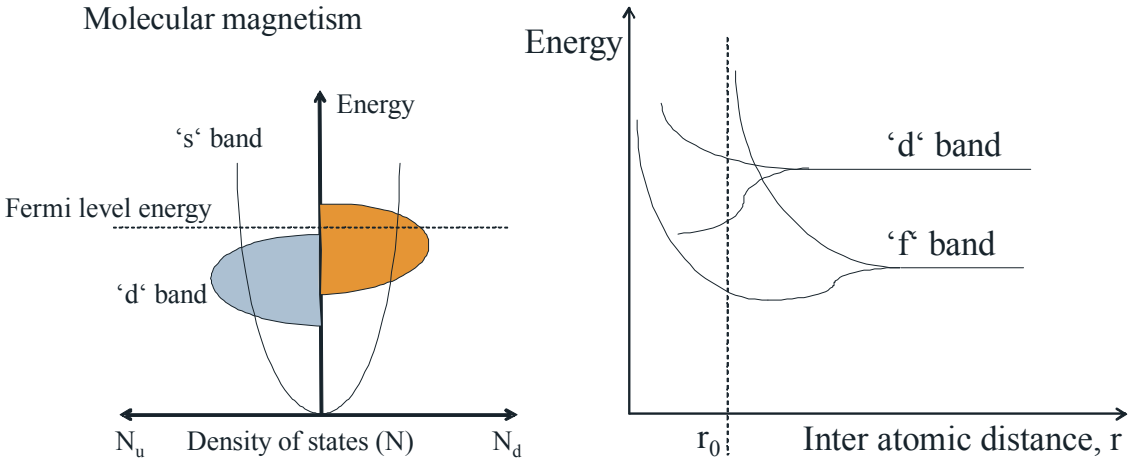


Figure 1.3: The first figure show energy band diagram of a ferromagnet and the second one signifies how 'd' or 'f' orbitals split when a molecule is closely bound in a crystal lattice, r_0 signifies interatomic spacing. Left one (N_u) signifies 'up' spin electron DOS and right one (N_d) 'down' spin electron DOS [33].

The mathematical relation between orbital magnetic moment (m) and angular momentum (l):

$$m = \frac{el}{2m_e}$$

or, m α l, proportionality constant is known as gyromagnetic ratio.

As orbital momentum is quantized (Bohr model), it can be written that,

$$m_z = -\frac{e\hbar m_l}{2m_e}$$

where $m_l = 0, \pm 1, \pm 2$ etc.
or, m α l, proportionality constant is known as gyromagnetic ratio. Here,

$$\hbar = \frac{h}{2\pi}$$

is the modified Planck's constant.

This begets to the concept of Bohr's magneton,

$$\mu_B = \frac{e\hbar_l}{2m_e}$$

hence,

$$m_z = m_l \mu_B$$

where, $\mu_B = 9{,}274.10^{-24}$ A-m^2.

Now, the mathematical relation between spin magnetic moment (m) and angular momentum (s) is,

$$m = -\frac{es}{m_e}$$

.

where, the spin magnetic quantum number is $m_s = \pm (1/2)$.

The component of spin along any axis is $\pm (\hbar/2)$,

So,

$$m_z = -\frac{e\hbar m_s}{m_e}$$

with $m_s = \pm (1/2)$.

Now, spin and orbit couple to give rise to a total electronic angular momentum (say, j) and this in turn generates the resultant magnetic moment. Several electrons in an atom generate magnetic moments (obviously a vector quantity) and they interfere with each other. An electron with 'up' spin can cancel magnetic moment of another electron in the same shell with 'down' spin. Any unpaired electron (in an unfulfilled shell, particularly the outermost ones) can produce effective magnetic moment of an atom. Again, assembling several atoms together breaks the energy bands and hence the magnetism is highly affected by interaction of outermost electrons. These are the primary understanding behind molecular magnetism.

Iron has electronic structure (Ar)$3d^6 4s^2$. So, there are 4 unpaired electrons (in 'd' orbital) and they should contribute to $4.\mu_B$ magnetic moment. When Iron solid is formed, '4s' orbitals of atoms overlap with each other to form a broad '4s' band, and '3d' orbitals to form a comparatively narrower band. They do overlap with each other and a charge transfer happens from '4s' to '3d'. In solid Irons, electronic structure becomes (Ar)$3d^{7,4} 4s^{0,6}$ ('3d' band has got spin configuration $3d_{up}^{4,8}$ $3d_{down}^{2,6}$ and hence number of unpaired electrons 2,2), and electrons occupy states with their magnetic moments either parallel or antiparallel to the ferromagnetic axis. So, bulk magnetization would be $2{,}2.\mu_B$. The same explanation is valid for metals like Nickel (bulk magnetization $0{,}6.\mu_B$), Cobalt (bulk magnetization $1{,}7.\mu_B$) [33] [29].

1.5.2.3 Magnetic materials:

The material magnetic behaviour is presented. The major terminologies pertaining to magnetism are to be kept in mind like paramagnetism, ferromagnetism (also antiferromagnetism), diamagnetism, ferrimagnetism and their features. Paramagnetic materials tend to produce an extra magnetic field as in the same direction as the externally applied magnetic field, so that the resultant magnetic field in the material goes higher compared to the externally applied field. Ferromagnetic materials have strong tendencies to align themselves even without the applied field. Permanent magnets are produced by these materials. So, relative permeability for paramagnetic materials are a little higher than 1 and for ferromagnetic materials are several hundreds or even more. One more important note is that ferromagnetic materials show hysteresis (ferromagnets can retain a memory of an applied field once it is removed). Diamagnetic materials show reduction of resultant magnetic field in them when placed in external field. Relative permeability is less than 1 or even negative. Actually diamagnetic substances are composed of atoms which have no net magnetic moments (say, all the orbital shells are filled and there are no unpaired electrons). Magnetic susceptibility (χ) is also an important property and is defined as the proportionality constant between magnetization of the material and magnetic intensity (for para and dia-magnetic materials). One thing is to be noticed is that paramagnetic materials does not retain the magnetic properties when external field is released [13][14].

Mathematical expressions of magnetic field:

$$B = \mu_0 (1 + \chi).H,$$

$$\mu_r = (1 + \chi),$$

so,

$$B = \mu_0 \mu_r H$$

where 'B' is magnetic induction (vector), I is intensity of magnetization, 'H' is magnetic field strength.
An increase in temperature (T) enhances atomic magnetic molecule randomization and henceforth decreases 'I' and 'χ' values. They bear a relationship as,

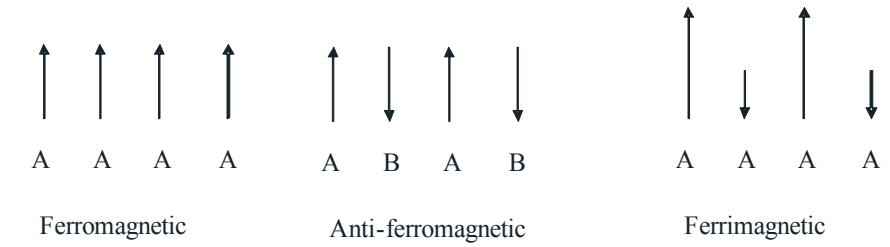
$$\chi = \frac{C}{T}$$

where C : Curie's constant.

At 'Curie point' temperature, a ferromagnetic material tends to behave as a paramagnetic one. Above this, 'χ' varies as,

$$\chi = \frac{C}{(T - T_c)}$$

where 'T_c' : Curie temperature.



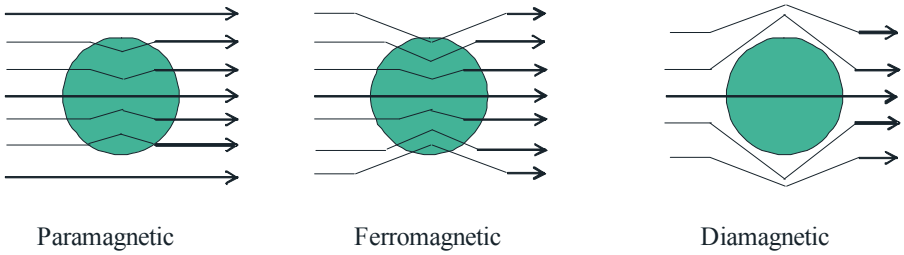


Figure 1.4: The figure shows that the differences between magnetic properties, magnetization orientation direction and others. Ferromagnetic material attracts magnetic field lines very strongly compared to Paramagnetic materials and the Diamagnetic materials have a tendency to repel somehow.

In antiferromagnetic materials, the adjacent ions or neighbouring spins or adjacent sublattices align themselves in antiparallel order (their magnetic moments are equal in magnitude) so that the gross external magnetism becomes almost zero. For ferrimagnertic materials, same phenomena happen, but opposing moments are unequal in nature so that resultant spontaneous magnetization remains. This spontaneous antiparallel coupling may disappear due to heating [14].
Among metals, Cobalt, Iron, Nickel show ferromagnetic properties. They are ferromagnetic at room temperature. Their alloys also show ferromagnetic properties. Magnesium, Molybdenum, Lithium, Tantalum and others show paramagnetism. The transition metals are observed to be paramagnetic (due to the presence of unpaired 'd' orbital electrons). Bismuth, Carbon, Mercury, Copper, water etc. show diamagnetic behavior. Again, Gold and Gold compounds generally show diamagnetic behaviour. Antiferromagnetism occurs in transition metal compounds, and metal like Chromium. Magnetite (Fe_3O_4) and Magnesioferrite ($MgFe_2O_4$) minerals show ferrimagnetic behave [33] [29].
Magnetite shows more than one type of crystal structures. In one of them, ‘Fe’ is surrounded by 4 ‘O’ ions and in the other model it is surrounded by 6 ‘O’ ions. These tetrahedral and octahedral sites form the two magnetic sublattices, and magnetic moments are not same in value and antiparallel with each other.
As this project uses Gold and Cobalt, all of these ideas would enhance better understanding.

1.5.2.4 GMR:

This is a type of magnetoresistance offered by thin film structures of alternating ferromagnetic and nonmagnetic films. Typical examples are Fe/Cr/Fe (Fe is ferromagnetic and Cr is antiferromagnetic at RT), Co/Cu/Co (one diamagnet in between two ferromagnets) and so on.

A brief description of the process is shown in the figures (ref: Figures 1.5, 1.6). Electrons can scatter (i.e. change their trajectory) for several reasons. Scattering can be electron spin dependent or spin independent. Again, electrons near the Fermi level energy only contribute to transport.

Spin polarization:

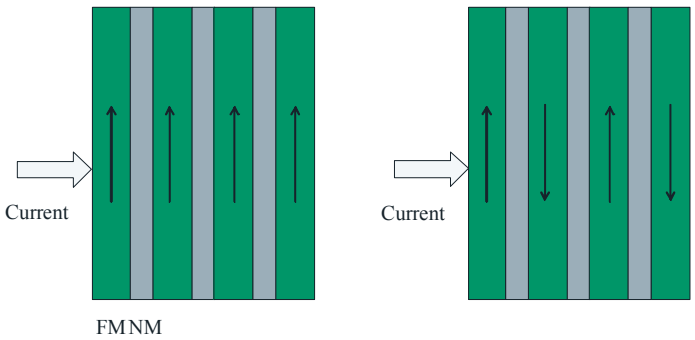
This is expressed as the ratio between DOS of 'up' and 'down' spins near the Fermi level and mathematically expressed as

$$SP = \frac{D_{up} - D_{down}}{D_{up} + D_{down}}$$

Paramagnetic materials have SP = 0 (i.e. 'up' spin and 'down' spin electrons are equal near Fermi level) and ferromagnetic materials have 0<SP<1. Temperature factor influences SP a lot. GMR or TMR performance is also known to be enhanced by using high spin polarized materials, hence using ferromagnetic materials with high SP at or above RT is very essential in spintronics science.

The resistances offered by the channel can be divided into two parts like bulk and interface resistances and also the spin 'up' and spin 'down' electrons would face different resistances (be it in interface or be it in bulk region). A high channel resistance signifies high probability of scattering and hence less current. The 'up' and 'down' spin electron channels would conduct parallelly. Now a current, spin polarized by the ferromagnet and passing through the non magnetic material, would remain polarized for the spin relaxation time duration. Spin relaxation time depends on the spin relaxation mechanism of the material. Again, thickness of the transport channel would play a significant role because if this be close to electron's mean free path, interface scattering would also become dominant.

At room temperature, Cobalt shows highest amount of spin polarization compared to other ferromagnets (Fe, Nickel). This is the primary reason behind the project's selection of Cobalt as the metallic electrodes. Gold could be used for proof of the principle that the downscaling of the structure would work or not [32] [33].



Parallel alignment of ferromagnetic (FM) followed by nonmagnetic (NM) material

Antiparallel alignment of ferromagnetic followed by nonmagnetic material

Figure 1.5: GMR materials are made from alternating layers of magnetic and non-magnetic metals that are nanometers in thickness

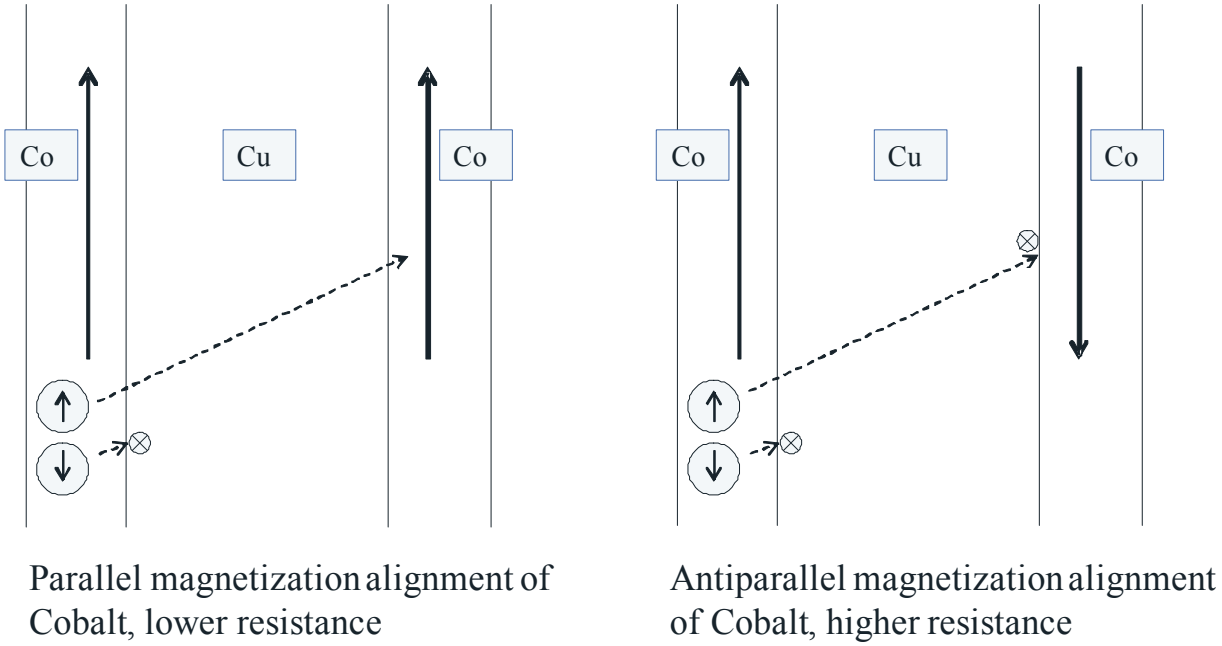


Figure 1.6: This picture describes GMR principle (Co/Cu/Co thin films). Bold lines show magnetization direction, circles show electron spin (so, some electrons are parallel and others are antiparallel with the ferromagnet's magnetization direction), dotted lines show electron transport, cross lines show spin scattering (especially in the interface region). The figure is self descriptive about the theory that electrons (from the spin injector, 'up' spin ones in the figure) would like not to contribute in transport if states with same spin are not available (on the spin detector side) or in other words if spin is opposite with magnetization direction [33]. The electrons (which are shown 'down' spin) always see a large difference in electron numbers between 'Cu' and 'Co' atoms and they are likely to scatter at the interfaces. These concepts describe the total phenomena.

1.5.2.5 TMR:

Two ferromagnetic layers separated by an electrical insulating thin layer (thickness typically less than 10 nm) exhibits tunneling magnetoresistance phenomena. The electrical resistance provided by the multilayered structure depends on the magnetization direction of the ferromagnets.
TMR effect is much higher than AMR or GMR. Some good examples of TMR would be Fe/MgO/Fe (200 % at RT), Fe/MgO/FeCo, CoFeB/MgO/CoFeB (600 % at RT and 1100 % at 4,2 K) etc. TMR decreases with increasing temperature and the bias voltage.

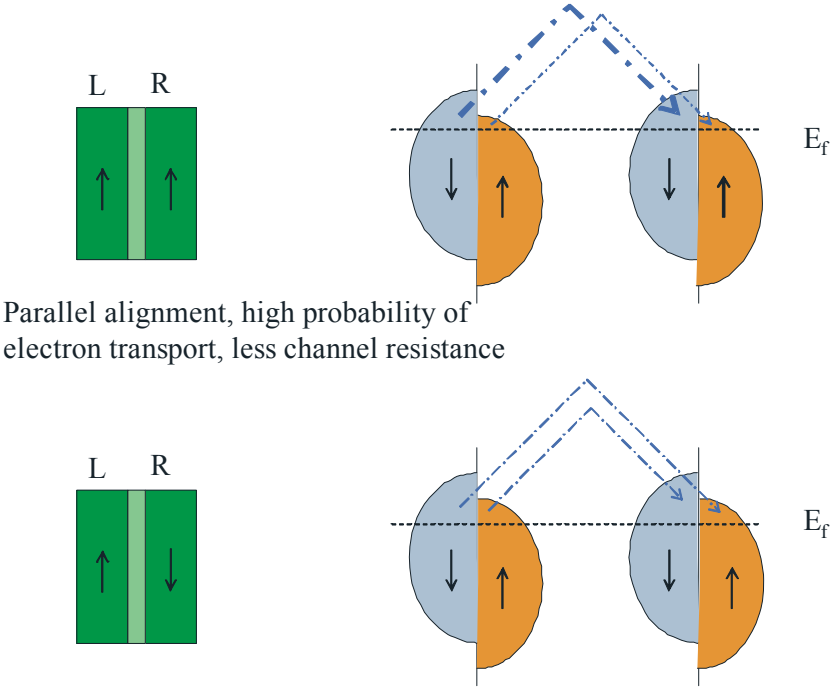


Figure 1.7: The figure shows energy band diagram and electron movement. First and the second pictures show two ferromagnets (magnetized consequently parallel and antiparallel with each other) separated by an insulator (ref: band diagram of ferromagnets mentioned before). 'E$_f$' signifies Fermi level energy; the arrows show electron transmission and bold font signifies high probability of transmission. So, in the second case, transmission probability is lesser than first one and hence their resistances differ accordingly. The principle of TMR is similar to GMR; the major difference being the electrons would 'tunnel' through an electrical insulator barrier (few nm) in TMR rather than get transported through a comparatively much higher channel length (hundreds of nm) electrical non insulator.

Julliene's theory behind TMR is discussed. In this theory, it is assumed that electron spin is conserved in the tunneling process and hence 'up' and 'down' spin electrons would form two different channels, with different channel resistances. Hence, the electrons from one spin state of one of the ferrromagnets would be accepted by an unfulfilled same spin state of the other ferromagnet. Refer to the figure. If 'FM1' and 'FM2' are magnetized parallel, minority spin electrons (from FM1) tunnel to minority (to FM2) and majority spin electrons to majority. If they are antiparallelly magnetized, minority spin electron would tunnel to majority states and majority to minority states. Conductance for a particular spin orientation would be proportional to the product of the effective DOS of the ferromagnets.

Mathemetical expression for TMR:

$$TMR = \frac{R_{ap} - R_p}{R_p}$$

Including spin polarization of ferromagnetic electrodes,

$$TMR \propto \frac{P_1 P_2}{1 - P_1 P_2}$$

where, 'P_1' and 'P_2' are the corresponding spin polarizations of the first and the second ferromagnets, 'R_p' and 'R_{ap}' are resistances in parallel and antiparallel alignment respectively.

A close equation about the change in resistance can be written as,

$$R_B = R_0[1 + m(\mu B)^2].\frac{\rho_B}{\rho_0}$$

'm' being length to width ratio, 'μ' signifies mobility, 'ρ' is resistivity (under or without the magnetic field, 'B') [33].

1.5.3 Utility:

Spintronics has huge application areas, as already being described. The major application is obviously in magnetic storage devices (mentioned in detail before) but in biology, spintronics can be use to detect cancer cells. Cancer cells are easy to be identified only when they are large in number. These cells when matured results in formation of tumor, which has to be removed by surgery. After surgery there may be presence of even a single cancer cell, which would result in growth of tumor in effected part of the body. The spintronic scanning is an efficient technique to detect cancer cells even when they are less in number. Spintronic devices are also used in the field of mass-storage devices. One of the most successful spintronic devices to date is the spin valve. This device utilizes a layered structure of thin films of magnetic materials, which changes electrical resistance depending on applied magnetic field direction. Spintronics may move forward to quantum information processing and quantum computing domain [17] [33].

1.6 The project view:

In this project, the major concentration is on developing the nanostructured devices (of varying geometry), integrating the spintronic functionality of molecules. This Masters thesis discusses all the results at the end and tries to make a concluding remark about the usability of the device. The project starts with some expectations and progresses with different assumptions and considerations. Some process steps has to be adopted keeping in mind that a series of modification would be required to improve the accuracy. The fabrication process starts with 10 number of wafers and a further 10 wafers were taken after a series of experiments. As trench dimensions will significantly influence the device performance, a set of different values for trench height and width are taken into consideration. The main challenges were to form the device (with proper dimension) and then check whether and how organic molecular channels are formed and how they can participate in the spin transport (may be a big space for future work). For filling up, different coating techniques are considered (like spin coat, spray coat and finally molecular beam deposition). For proof of proper fill up, electrical measurements (any kind of short or open circuit) were used at relevant steps and even some wafers are broken up for SEM images. So, in the project's design part, Layout editor is used (MEMS/IC fabrication software). During fabrication steps, the deposition parameters were chosen based on different SEM images. All the measurement data and results are tabulated and an overview is presented at the end about the success of the work.

2. Project task

This part of the project belongs to 'Towards Molecular Spintronics' (TMS) research unit. The major aim of the TMS group deals with the ultimate down-scaled nanostructured device integrating the spintronic functionality of single molecules. An attempt would be made to switch the spin transfer through magnetic molecules by changing the alignment of the molecular spins. This notion would demand an involvement of both of the two branches of science, organic electronics and molecular magnetism.
TMS encapsulates different aspects like magnetic molecule characterization, fabrication of molecular thin films followed by device realization, on chip integration and others. This research group encompasses several research units and this thesis is a part of them. The major aim of the thesis has been to fabricate the laterally stacked device using SCREAM technology and reach a series of dimensions where the spin transport could be analyzed best. The transport channel is to be composed of thin films of magnetic molecules. The spin transport medium can be of different organic semiconductors like Phthalocyanines ('CuPc', 'MnPc', FePc etc), pentacene ($C_{22}H_{14}$), polyacetylene (polymers, $(C_2H_2)_n$) and poly-di-acetylene, 'C_{60}' (fullerene) etc (transport could also be studied in Quantum dots or nanowires, graphene structure or graphite structure, some self assembled molecules etc.). C_{60} is typically a caged 'C' structure and caged 'C' group show strong colour as well (C_{60} is magenta, C_{70} is reddish yellow etc) [35] [36]. The project would deposit 'CuPc' for the first set of results.

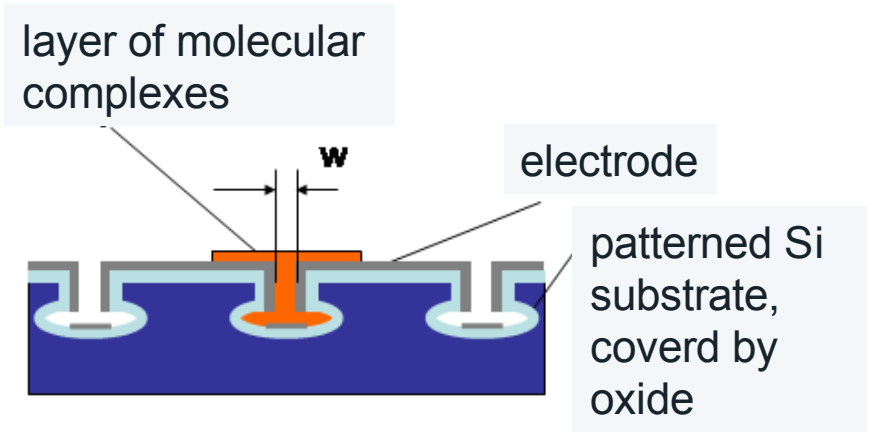


Figure 2.1: Picture showing the transport phenomena, used for this project

Tasks:

Tasks for the thesis has been to design and fabricate structured substrates for laterally stacked inorganic or organic devices by photolithography, Silicon etching, oxide and metal deposition.

1. Development of technological concepts, develop technology flow diagram.
2. Design and layout of different geometries based on trench isolation technology.
3. Supervision of device fabrication with focus on trench width adjustment.
4. Optical characterization of the trench devices (microscopic images).

5. Coating of organic magnetic material by OMBD.
6. Characterization of filled devices.
7. Test of alternative coating processes.

As mentioned earlier, spin transport can be realized in different geometries and in various directions like lateral or vertical. Even the lateral transport can be realized in various ways. Fig: 2.1 shows the model this thesis follows and other possibilities are noted down in the Appendix section.

3. Device geometry

This part of the thesis concentrates on dimensions of trenches and device geometries. As it was mentioned earlier, the trench dimensions would be varied (also, the electrode geometry). Initially some different units are planned and then the total structure is designed. This chapter is divided into some sections with images for a better understanding.

3.1 Basic Units:

The device consists of the silicon wafer, with deposited oxide on its top and the metal electrodes. The dimensions of the oxide followed by metal depositions are fixed later. Two basic structural geometries are defined like 'type 1' and 'type 2'. For 'type 1' structures, the metal electrodes are chosen to be perfect square, and the 'type 2' structures are of different geometries as shown in the figure (and thus a comparison between the results of these two geometries could be made). The next step is to develop the trench geometries. The wafer would consist of several trenches with different openings (800 nm to 1000 nm are the trenches of the interest and 5 um, 10 um width trenches to isolate different structures from each other. From now and onwards, the term 'trench' would signify only the trenches of project's interest, not the isolating ones). The trench dimension (less than 1 um) would play the most significant role as the main focus is on the organic molecule deposition in the trenches. A certain naming convention is provided in the table, a particular name relates to a certain structure (like structures named 'A1' have trench length (t_l) of 10 um and trench isolation width (t_w) 800 nm. Also, this very structure uses 'type 1' geometry. The same dimension with 'type 2' geometry gives rise to 'A5'). So, 1,2,3,4 structures have 'type 1' geometry and 5,6,7,8 have 'type 2' geometry.

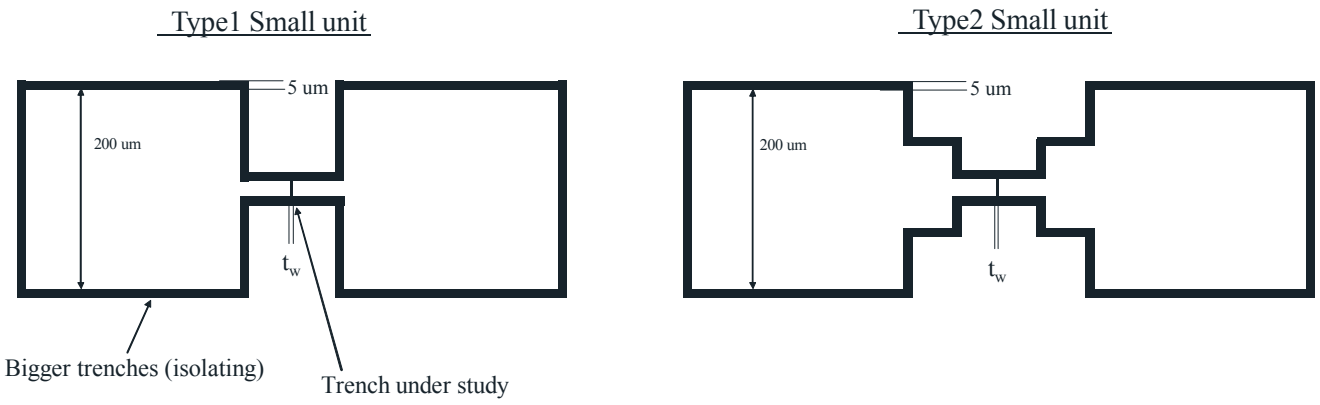


Figure 3.1: Picture showing different units and trenches

The minimum trench isolation width is kept as 800 nm and vary this by 20 nm to generate 11 different structures. The maximum width is kept as 1000 nm. By this way, it is ensured that even if one can not keep a significant final trench opening for organic molecule deposition for the smallest structures (this might happen due to deposition uncertainties, because if one would try to deposit the oxide followed by metal in nm range, a small variation in deposition parameter might influence a lot), the bigger trenches would be there for fill up. The trench length is also varied as 10 um, 20 um, 30 um, 40 um. By this way, a test for spin transport on

different geometries would be possible. One has to break some of the samples to reach a structure as perfectly as possible and rely on SEM images to decide how much oxide and gold should be deposited.
So, 11 times 4 = 44 structures would be generated for each type (‘type 1’ and ‘type 2’) and these contribute to 88 different geometry structures in total. By this way, one can proceed further to form the wafer grid. The below mentioned table includes all the possibilities.

Table of units:

Type 1- Geometry:

Trench isolation width, t_w (nm)	Trench length, t_l (um)	Names	Total units	Small unit dimension (um)
800	10,20,30,40	A1, A2, A3, A4	44	L=850, W=500
820	10,20,30,40	B1, B2, B3, B4		
840	10,20,30,40	C1, C2, C3, C4		
860	10,20,30,40	D1, D2, D3, D4		
880	10,20,30,40	E1, E2, E3, E4		
900	10,20,30,40	F1, F2, F3, F4		
920	10,20,30,40	G1, G2, G3, G4		
940	10,20,30,40	H1, H2, H3, H4		
960	10,20,30,40	I1, I2, I3, I4		
980	10,20,30,40	J1, J2, J3, J4		
1000	10,20,30,40	L1, L2, L3, L4		

Table (i): This table includes all the design dimensions for ‘type 1’ geometry

Type 2- Geometry:

Trench isolation width, t_w (nm)	Trench length, t_l (um)	Names	Total units	Small unit dimension (um)
800	10,20,30,40	A5, A6, A7, A8	44	L=960, W=500
820	10,20,30,40	B5, B6, B7, B8		
840	10,20,30,40	C5, C6, C7, C8		
860	10,20,30,40	D5, D6, D7, D8		
880	10,20,30,40	E5, E6, E7, E8		
900	10,20,30,40	F5, F6, F7, F8		
920	10,20,30,40	G5, G6, G7, G8		
940	10,20,30,40	H5, H6, H7, H8		
960	10,20,30,40	I5, I6, I7, I8		
980	10,20,30,40	J5, J6, J7, J8		
1000	10,20,30,40	L5, L6, L7, L8		

Table (ii): This table includes all the design dimensions for ‘type 2’ geometry

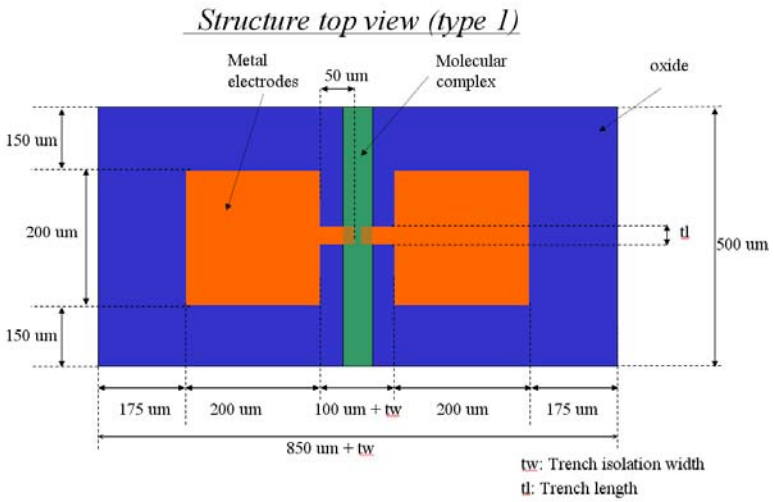


Figure 3.3: Image showing complete geometry of the 'type 1' structures, with all the exact dimensions being used for this project

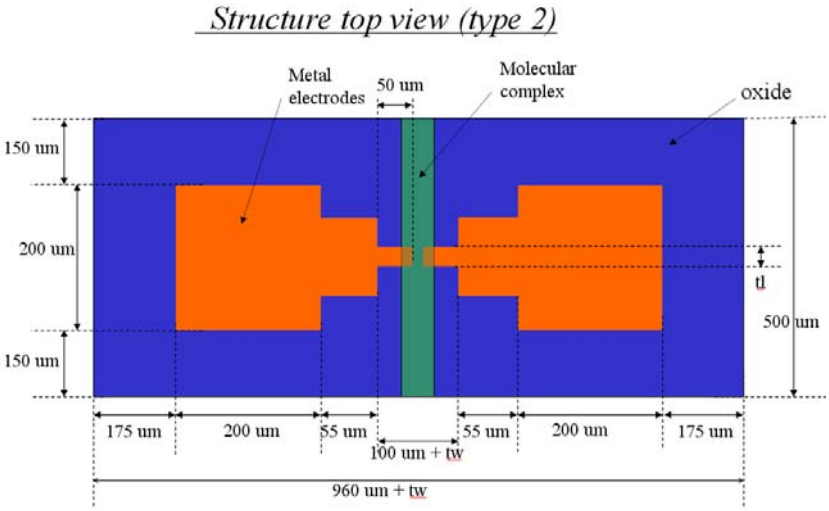


Figure 3.4: Image showing complete geometry of the 'type 2' structures, with all the exact dimensions being used for this project

3.2 Design:

The design is made on basis of these values and considerations. The design software used is 'Layout editor'. The first step was to design the 'type 1' electrode with proper dimensions (A1) followed by 'type 2' (A5). Afterwards, the dimensions are varied to generate all the other units (like 'A2' or 'A6' etc., followed by 'B', 'C' and the rest). A proper sketching is provided to have a complete understanding of different structures. Henceforth a single large unit is developed consisting of 88 small units (ref: Appendix). Several large units are built to form the wafer grid. The main challenge during this part of the project was to keep proper dimensions because they are in nanometer ranges. Looking at the wafer grid one would note that three test fields are created, some of the measurements would be done in this region only rather than going for the total wafer. The important point is that each structure has its name on

its top even in its layout (ref: wafer layout images provided in the Appendix), so that it would be quite easier to identify them after breaking the samples.

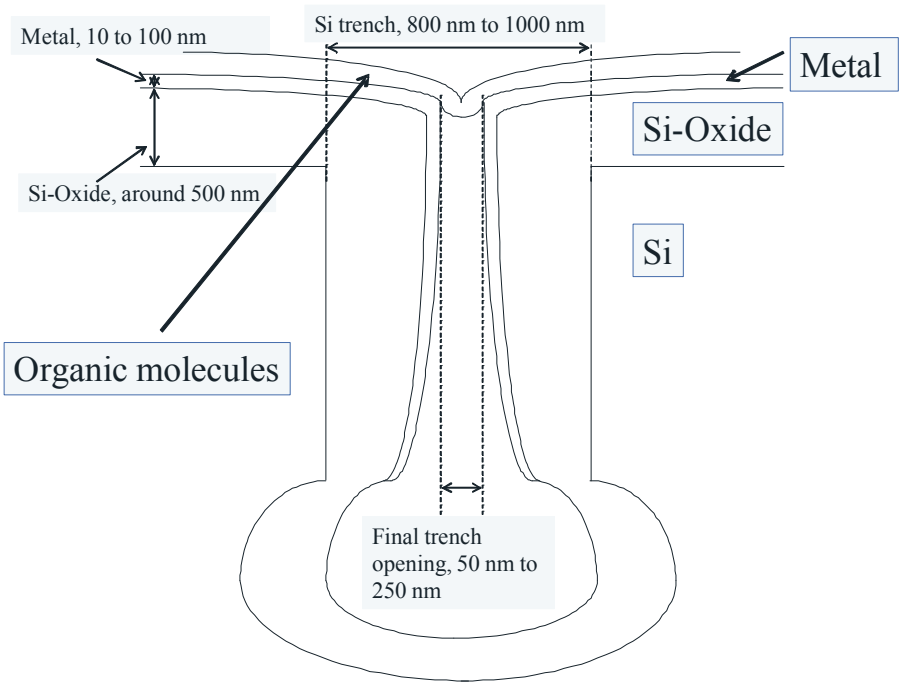


Figure 3.5: Picture showing typical cross sectional view of one of the trenches with near perfect dimensions

4. Fabrication Process:

This section illustrates the overview of the several process steps essential for the micro fabrication world like lithography followed by different other processes like high aspect ratio trench formation, a provision to nullify the short circuit possibilities between two electrodes and followed by the oxide and metal deposition in nanometer range. Following the necessary process steps, the devices are formed. At the end, an attempt to deposit the organic material would be done in the trenches for analyzing the spintronic property. All of these processes (along with the following measurement steps discussed later) were accomplished in the cleanrooms of Technical University of Chemnitz, 'Zfm' and Fraunhofer 'enas' institute (also in 'Physics' department for sputtering and OMBD). This chapter has several parts for a better understanding on the device fabrication with one of the major image of this research, the process flow. All the processes (like 'Etching', 'CVD', 'PVD' and others) are described as well in brief because a theoretical idea will improve the practical understanding. The reaction chemistry, process parameters are also mentioned to elaborate what actually happens to get the outcome.

4.1 Lithographic mask-reticle generation:

For the lithographic mask, reticle used as 10:1 and used mask dimension is (5 inch) times (5 inch) times (0,09 inch). This is generated on the basis of the wafer layout discussed earlier.

4.2 Formation of oxide mask layer:

The SiO_2 mask layer is developed on the wafer by Thermal oxidation. Deposition thickness is 500 nm. The next steps would be cleaning followed by the temperature treatment.

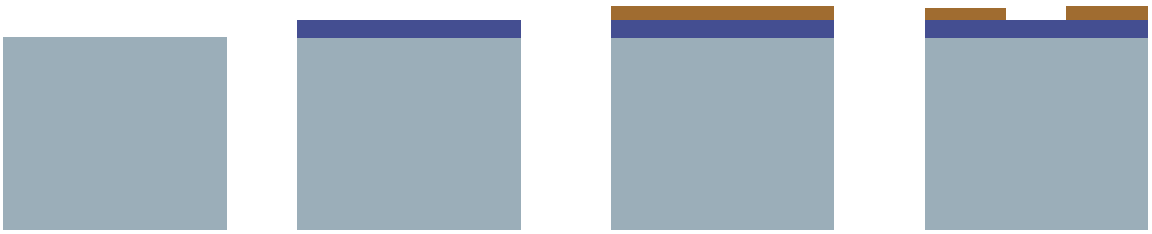
4.3 Lithography or pattern transfer:

Lithography is the process of pattern transfer into a resist (reactive polymer film) from a predesigned mask. There are different types of lithography processes, using various lens systems and exposure radiation sources.

The project starts with projection (stepper) lithography. A minimum of 800 nm (theoretically) trench opening could be achieved in the laboratory by this process (as already being mentioned in the design, in fact the design was done accordingly), but a use of nanolithography could give smaller values. Nanolithography was not available and hence projection lithography is used and a further reduction of trench opening would be done (to count for the spin transport phenomena, one needs to have smaller trenches, typically transport length should be less than 300 nm) by depositing oxide on it.

Specifications for the used lithographic process:

- Resist: OiR 906-12 Ca. 1,3 um.
- Exposure: 2,4 s.
- Exposure of the whole wafer (flood exposure): 60 s.

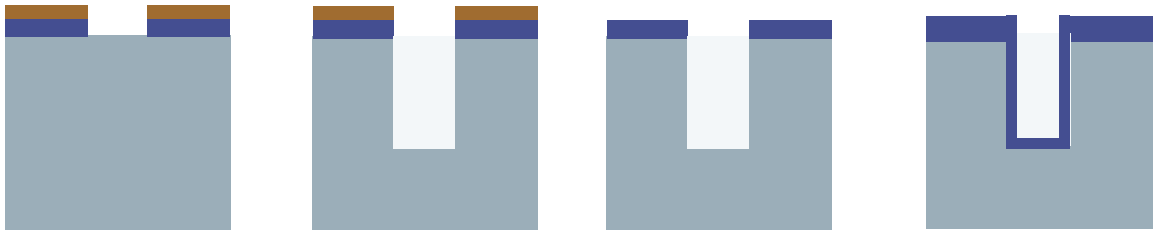


1. Silicon wafer

2. Deposition of oxide mask layer

3. Wafer with Lithographic resist

4. Pattern transfer by Lithography onto the wafer



5. Oxide mask Restructuring by Anisotropic etching

6. Silicon Deep Reactive Ion etching

7. Removal of resist

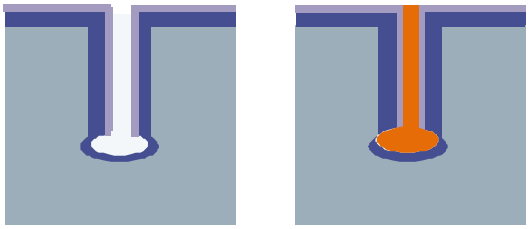
8. Spacer oxide deposition by PECVD, to protect the sidewalls

9. Spacer oxide etching to open the trench bottom

10. Isotropic silicon etching (for metal electrode deposition)

11. Complete oxide removal by wet etch

12. Trench refill by further oxide deposition to reduce the trenches to around 200 nm (TO/LPCVD)



13. Sputter deposition of metal electrode film

14. Deposition of organic Molecules for Spintronics analysis

Figure 4.1: This self explanatory picture depicts the process flow

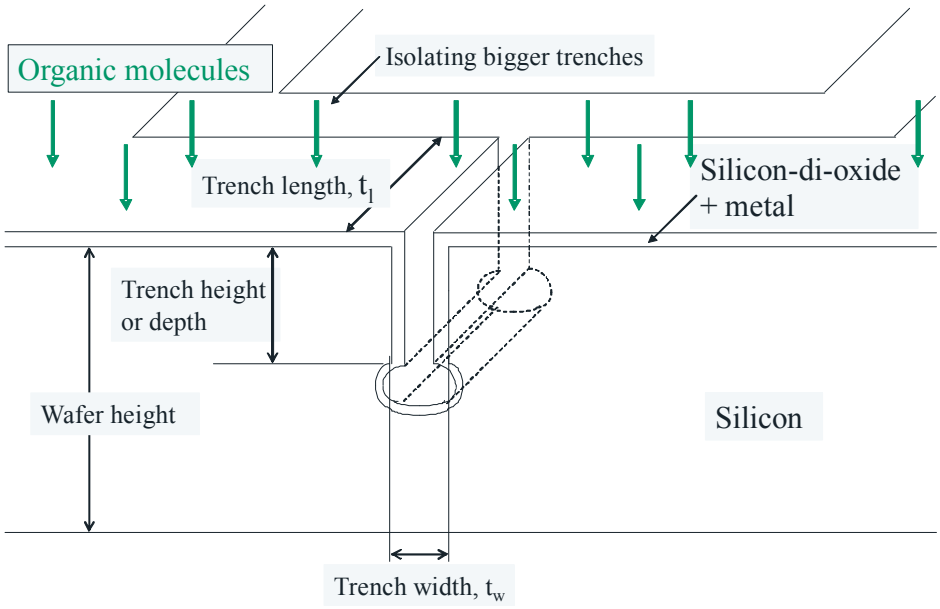


Figure 4.2: The image shows 3D geometrical view of the structure used for the project

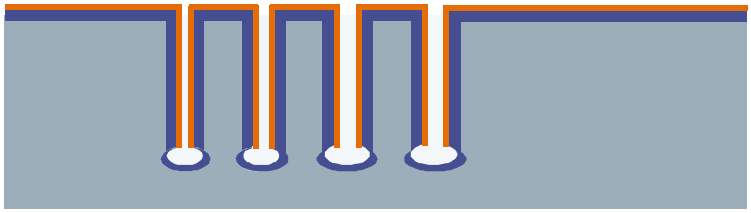


Figure 4.3: The picture showing 4 different trenches of varying width with the oxide and metal on the top

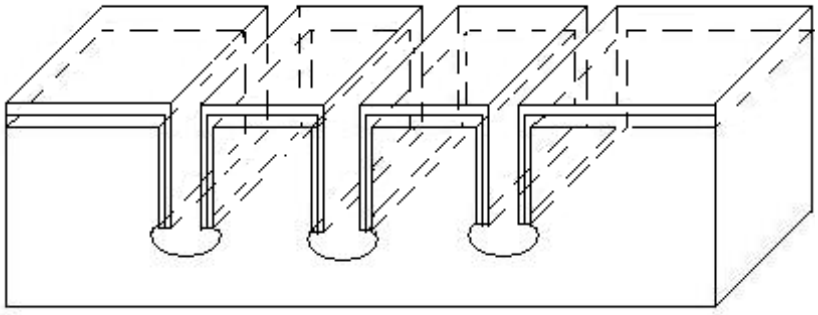


Figure 4.4: This picture shows another 3D image showing 3 trenches, Silicon with a layer of oxide and another layer of metal

4.4 Oxide mask restructuring:

The basics on etching processes are noted down. Based on this understading, different etching process would be used in the project and their importance would be discussed.

4.4.1 Etching in general:

In wafer fabrication processes, etching signifies the removal of a part of any material (like Silicon, oxides, nitrides, photoresists etc). Photoresist masks are used on the wafer for pattern transfer, so that the materials, not covered by the mask, get etched away. Etching process can be classified into several types like,

Dry etching: This does not utilize any liquid chemicals/etchants to remove material from the wafer. Dry etch can be of both isotropic and anisotropic ones. Dry etching may be only physical process (like sputtering; anisotropic) or chemical process (Barrel etch; isotropic) or both at the same time (like RIE, plasma etch). Typical etchants used are SF_6, CF_4, NF_3, Cl_2 gases, depending on material to be etched. This technology is expensive.
Wet etching: This utilizes liquid chemicals to remove material from the wafer. Generally this process is isotropic one. Common etchants used are KOH solution, HF solution, H_3PO_4 solution, again depending upon the material to be etched away.

Some more terms in etch chemistry,

Isotropic etching: When the etching rate is same in all direction. This type of etching is highly selective.
Anisotropic etching: Etching rate is direction sensitive. The material is etched away in either (lateral or vertical) directions.
Underetching: When some part of the material under the mask gets removed as well.
Etch rate: The amount of material cleared away per unit time, generally in Armstrong (or nm) per second. This term depends on temperature and surface activation energy.
Etch selectivity: This is the ability of the reacting species to etch away only the material of our concern leaving other materials unharmed. So, one can define selectivity (S) as,

$$S = \frac{R_{film}}{R_{substrate}}$$

'R' being etch rate.
Or, even,

$$S = \frac{\varepsilon_{film_1}}{\varepsilon_{film_2}}$$

S >> 1 is desired.

Degree of anisotropy: This term is defined as,

$$A = 1 - \frac{R_l}{R_v}$$

'R_l' is lateral etch rate, 'R_v' vertical etch rate.

For perfect anisotropic etching, A = 1, (as $R_l = 0$). For perfect isotropic etching, A = 0 (as $R_l = R_v$). In general,

$$0 < A \leq 1.$$

4.4.2 The process:

Here, the oxide mask is anisotropically etched away (ref: The process flow diagram. The process must be anisotropic otherwise wrong dimension would be transferred during the trench formation) to make the opening at the top necessary for the next step, i.e. the deep etching of silicon (as the next step incorporates DRIE of 'Si' in selective parts of the wafer, this step is very important to get rid of oxide from these parts). A measure of the etching depth is necessary to ensure whether or not the oxide is removed perfectly. Dry etching process was chosen as wet etching is generally isotropic.

Process parameters:

- Etch process: Dry etching.
- Gases used: 15 sccm CHF_3 and 18 sccm CF_4.
- Etching time: 3min 30 sec.
- Etch depth: around 500 nm.
- Used pressure: 7 mTorr or 933,25 mPa.
- ICP power: 1300 Watt.

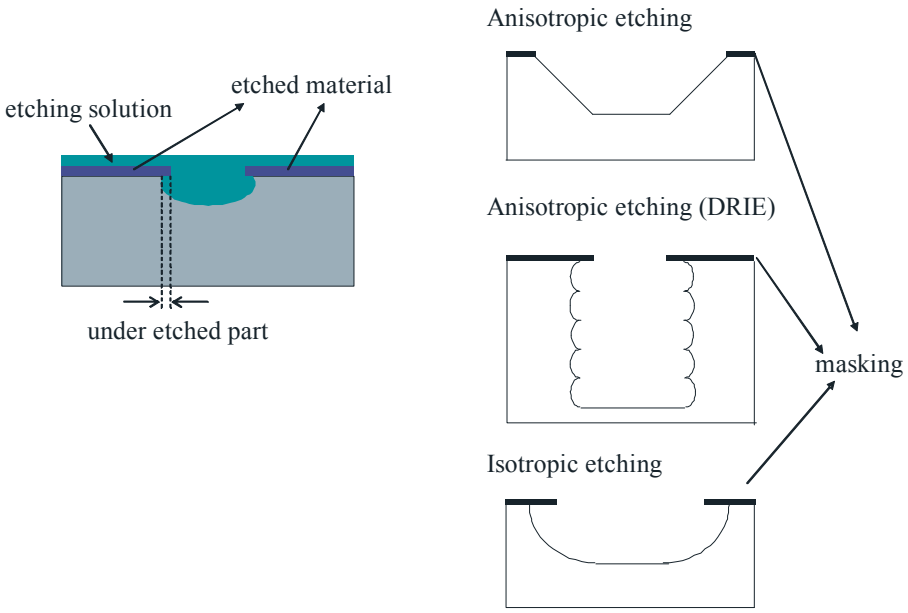


Figure 4.5: Picture shows typical etching profiles of the structures, showing underetching, isotropy or anisotropy etc

Process reaction:

SiO_2 (solid) + CF_4 → SiF_4 (gas) + CO (gas).

4.5 Deep anisotropic silicon etching:

This is one of the major technological steps to form the trench. The trench depth for different wafers are kept different (3 um, 6 um, 9 um, 5 um) and they will be discussed later in details (One point is to be noted that if the trench depth differs, the organic molecular channels would be formed in different ways and the spin transport length and nature would be influenced).

A very nearly isotropic plasma etching 'Bosch' process is used. High density plasma source is used, 'Bosch' process uses (i) a fluorine based plasma chemistry to etch the silicon (ii) the fluorocarbon group to provide a sidewall passivation as well. A passivation layer is made to form to protect the entire substrate from further chemical attack. A complete etch process therefore encompasses both etching and deposition steps. A high density plasma (one of the widely used technology is ICP) makes the reacting gases break down (produces 'F' radicals from SF_6 compound) before coming in touch with the wafers. 'Bosch' process shows higher etch rate with good etch selectivity. Modern technology can achieve an etch rate of even higher than 20 um/min. A higher etch rate would cause roughness in the side walls so a compromise should be drawn by the user. A high etch rate would also demand a higher flow of process gases and thus a fast pumping. [27] [28]

Process parameters:

- Etch time depends on the trench depths.
- Mean process pressure: 15 mTorr or 2 Pa
- ICP power: 600 W (a higher etch rate demands more ICP power)
- Chiller temperature: 20 °C
- Helium back pressure: 1.3 kPa
- RF bias: 12 Watt
- Gases used: SF_6 and120 sccm C_4H_8
- Etch time: less than 10 sec depending on the trench depth

Process reactions:

1. Dissociation: C_4H_8 → 4 CF_2 Polymerization: nCF_2 → $(CF_2)_n$: for passivation
2. Dissociation: SF_6 → F^* + S^* Etch reaction: Si + F^* → SiF (gas) : for etching

The next step is removal of the redundant photoresist and the cleaning.

4.6 Side wall passivation by PECVD:

4.6.1 CVD in general:

Chemical vapour deposition is a chemical deposition process to produce pure solid materials. Precursor is used which react with the substrate and deposit on it. There is another process named physical vapour deposition which use purely physical processes like evaporation or sputtering or cathodic arc deposition etc.

CVD involves gas phase reactions on the surface. Gas phase reactions are very much dependent on temperature and pressure parameters of the reactants.
Chemical vapour deposition can be of different types (based on application pressure and temperature, also on reactant used), like APCVD (deposition temperature is around 900 to 1200 °C), LPCVD (deposition temperature is lower like 600 to 800 °C, pressure is low), PECVD (temperature even lower because of use of the plasma), ALD and so on.

4.6.2 PECVD:

Typical temperature varies in between 200 to 500 °C. The plasma is ignited in between two electrodes, either by RF or DC discharge. This technological step is necessary because sidewalls are needed to be protected from being isotropically etched away because in the next to next step, the trenches (only the bottom) are to be etched isotropically. If one skips this step, then the total trench would be etched isotropically.

List of parameters:

- Deposition temperature: 350 °C.
- Deposition pressure: 850 mTorr.
- Deposition thickness: 200 nm.
- Deposition rate: 29,2 nm/min.
- Gases used: 3% SiH_4/N_2 (gas 1), N_2O (gas 2).

Process reaction:

$$SiH_4\,(gas) + 2N_2O\,(gas) \rightarrow SiO_2\,(solid) + 2H_2\,(gas) + 2N_2\,(gas)$$

4.7 Spacer etching:

This part of the fabrication process is done to erase the oxide layer from the trench bottoms so that in the next step, only silicon would be left at the bottom of the trench. The etch rate is an important criteria for this process to make sure that the oxide is removed completely.
ICP etching (anisotropic) process is used for this step. A high etching rate may be obtained by higher ion density. The Oxford Plasmalab system 100 ICP-RIE machine is used (this machine provides a high range of temperature of the substrate electrodes, like -150 to 400 °C. Used ICP is of 200 Watt). The ions are made to drift towards the wafer substrate where they would collide with the sample substrate (positively charged) to be etched.

List of parameters:

- Etching pressure: 5 mTorr (666,6 Pa)
- Etch thickness: 200 nm.
- Etch time: around 2 min 30 secs.
- ICP Power: 200 Watt.
- Gases used: 20 sccm CF_4.

Process reaction:

$$SiO_2\,(s) + 4F + 2C \rightarrow SiF_4\,(g) + O_2\,(g)$$

4.8 Isotropic silicon etching:

This step is one of the important steps in this project. If this processes is omitted, there will be short circuit of metallic contacts (would be deposited later). This step helps to separate two metal electrodes.

List of parameters:

- Etching pressure: 4 KPa.
- 'He' back pressure: 1,3 KPa.
- Etch time: 20 secs.
- Etching type: Dry etch.
- ICP Power: 800 Watt.
- Chill temperature: 20 °C.
- Gases used: 130 sccm SF_6 + 13 sccm O_2

Process reaction:

SiO_2 (s) + F^* → SiF (g) + by products

4.9 Oxide removal:

In this project, the oxide is to be deposited (to make the trenches narrower) by more than one procedure so that one can decide which one would fit well as per requirement. The final aim is to study spin transport phenomena (near the surface and inside the trenches) in certain geometry at the nanometer scale. Different processes have different deposition characteristics and a decision can be made on the deposition procedure to be fitting most, and also the amount of deposition. The oxide deposited by PECVD in last steps is completely removed wet chemically and a new layer of oxide is deposited.
Two major processes like thermal deposition and LPCVD are chosen for this. The amount of deposition will differ for them (reason is described in the following sections). Total oxide is removed wet chemically to leave behind the naked silicon trenches.
The next step would be cleaning of the wafers.

4.10 LPCVD or Thermal oxidation:

This deposition technique provides,

(i) Electrical insulation from both sides between Silicon and the metal (to be deposited in the following sections).
(ii) Lowers the trench opening from a minimum value one can get from the lithography (as mentioned before) avaiable. This very process majorly takes care of the spin transport length of the final device. A control over this process is one of the essential requirements of this project.
(iii) This is responsible to form a capacitance between the deposited metal and the silicon.

4.10.1 LPCVD:

In this process, the pressure is kept like 0.01 to 10 mbar with temperature around 600 to 800 °C or little more. This process is used to deposit poly-silicon, silicon dioxides, silicon nitrides etc. in thin film technology. Some wafers are chosen for this step.

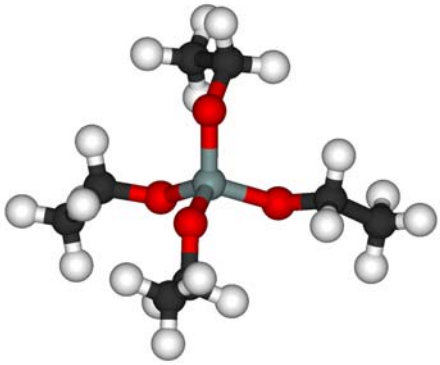


Figure 4.6: Chemical structure of TEOS ($Si(OC_2H_5)_4$) molecule. The gray molecule is Si, red one is Oxygen, black ones are Carbon and light gray ones are Hydrogen.

TEOS-LPCVD is being used in industries for several years with well established equipments. This method is advantageous compared to other existing methods in terms of low production cost, low stress etc. For this project, this process will be favoured, and the major reasons are good conformality (this is an important criteria as very narrow trenches would be filled up) and high breakdown voltage of the deposited oxide.
The amount of deposition would be discussed in the results section as a decision is to be made based on SEM images (mentioned before).

List of parameters:

- Deposition temperature: 725 °C.
- Deposition pressure: 215 mTorr or 28,66 Pa.
- Deposition rate: 10,3 nm/min.
- Reactants used: TEOS (130 sccm), O_2 (100 sccm).

Process reactions:

Gas phase: $Si(OC_2H_5)_4 \rightarrow Si(OC_2H_5)_3OH + C_2H_4$.
Surface: $Si(OC_2H_5)_3OH \rightarrow SiO_2 + 2H_2O + 3C_2H_4$.

4.10.2 Thermal oxidation:

Thermal oxidation is another kind of deposition technique used in Microtechnology. Here, the aim is to deposit the thin layer of Silicon dioxide on the surface of the silicon wafer. Oxygen diffuses into the wafer if treated at high temperature and reacts with the surface. This might happen both in dry condition and in wet condition, depending on the usage. Again, some wafers are chosen for this process.

List of parameters:

- Deposition temperature: 1000°C.
- Deposition pressure: 1 atmos.
- Deposition rate: 3,45 nm/min.
- Gases used: O_2 (6 slm), H_2 (10 slm).
- Oxidation type: wet.

Chemical reactions:

Si (solid) + $2H_2O$ (vapour) → SiO_2 (solid) + $2H_2$ (vapour) : wet oxidation
Si (solid) + O_2 (vapour) → SiO_2 (solid) : dry oxidation

Some notes:

1. Thermal oxide grows both at the top and the bottom of the Silicon wafer layer, approximately 46% lies below the original surface and rest 54% above it. This theory is known as 'Deal Grove' model of TO.
Mathematically,

$$X_{Si} = X_{ox} \cdot \frac{N_{ox}}{N_{Si}}$$

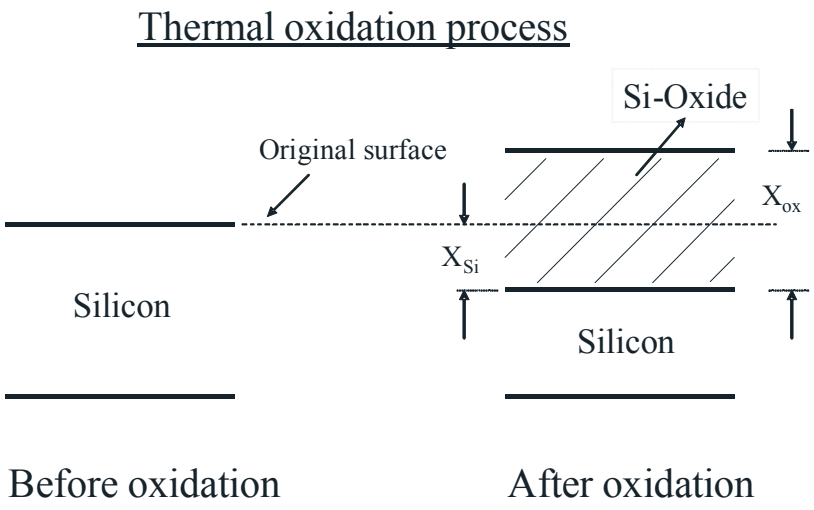


Figure 4.7: Typical Thermal oxidation profile

where 'X_{Si}' signifies the part inside the actual Silicon surface and 'X_{ox}' means the total oxide thickness, as shown in the figure [37].

2. Oxidation rate of silicon is a function of the crystal orientation of the silicon surface, <111> wafer grows better than <100> etc.

3. Oxide growth rate goes slow with a lowered temperature.

4. Oxide thickness depends somewhat on radius of curvature of the silicon surface. The smaller the radius, thinner will be the oxide.

5. Wet oxidation process is preferred as growth rate is higher for wet oxidation process compared to dry one, but when film's optical/magnetic properties play a significant role, one can opt for dry process.

6. Density depends on the structure of SiO_2, amorphous (2,21 gm/cc) or crystalline (2,65 gm/cc).

7. Oxide Growth Rate slows down with increase oxide thickness [17] [37].

4.11 Metallization:

This part is done by sputtering. By colliding accelerated ions with the target material, it is possible to knock atoms out of the target. The sputtered atoms and ions have wide range of energy distribution and they fly from the target (Cobalt) to the substrate (the samples). The deposition rate might vary from fractions of nanometers to several. The nominal thickness can even be of a monolayer. A turbo pumped high vacuum is created in the main chamber with the necessary base pressure. For this experiment, inert gas like 'Ar' is used to prevent reactions with deposited material. DC magnetron sputtering is used where a fixed bias voltage between the target and an anode is applied. The anode is ring shaped around the target to obtain a localized electric field. The accelerated electron between the target and the anode lead to an ionization of the sputter gas. In order to contain the ionized gas a radially symmetric magnetic field is applied from below the target (refer figure). The plasma torus that is formed this way will only touch the target surface on a small ring shaped area where sputtering takes place. Those knocked out atoms and atom clusters that have a total charge of zero are not affected by the applied fields and will form a cloud extending into the vacuum and eventually onto the substrate surface.

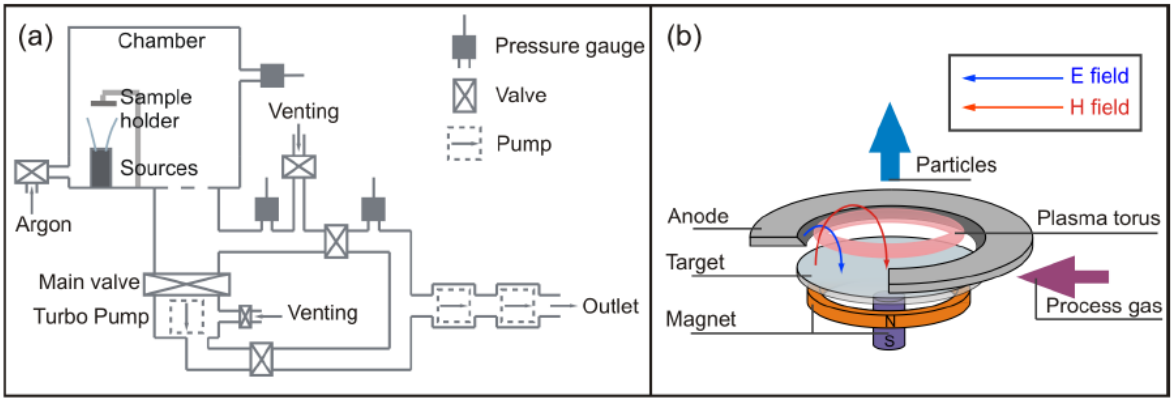


Figure 4.8: Panel (a) shows a schematic view of the sputter system *B55* used for the deposition of all the layers. Panel (b) shows the magnetron source in greater detail.

Cobalt deposition parameters (100 nm):

- Base pressure: 10^{-6} mbar.
- Argon pressure: $3{,}5.10^{-3}$ mbar.

- Deposition rate: 0,05 nm/sec .
- Nominal film thickness: 100 nm.
- Nominal film thickness measurement process: Quartz thickness monitor
- Temperature: RT

4.12 Organic molecule deposition:

The organic molecular beam deposition is another thin film growth process especially for large organic molecules. OMBD incorporates evaporation of molecules by thermal heating system in a low pressure chamber, and finally depositing onto a substrate in crystalline form. By this way, it allows the growth of complex layer sequences with a defined thickness of various organic semiconductors in combination with dielectric films, different metallizations, and indium–tin oxide layers. Generally, the growth rate ranges from 1-5 nm/min (for the project, it is around 1 nm/min). Copper Phthalocyanines is used as the organic material, the different specifications are noted down,

(a) Substrate Temperature : 320-345 °C
(b) Substrate Pressure : 1,5 – 2,2 ($x10^{-7}$) mbar
(c) Growth type : Polycrystalline
(d) Current : 1,24 Amp
(e) Voltage : 4,0 Volt
(f) Frequency rate kept : 10-12 Hz/min (growth rate is near 1 nm/min)
(g) Frequency shift : 2000 Hz
(h) Time taken : 3 hrs

The pressure is reached by using both mechanical pump and turbo pump. Two different chambers (inner and outer) are used, along with a separating valve. The depositing material (CuPc) is kept inside the inner chamber and pressure is pulled down low as like the substrate pressure. Electrical connection is provided to heat CuPc (the temperature is reached by using electric current). The sample is inserted in the outside chamber and pressure is reduce to around $1x10^{-6}$ mbar. The growth is measured by a microbalance system. Whenever the molecules grow on the substrate, its mass increases and this is detected by the electronic system. A change in mass will be reflected in a change of frequency. Initially the the growth rate is fixed by manipulating the heating current to a certain value (as shown above, the growth rate is very sensitive to the heating current), and afterwards I start deposition on the desired substrate by inserting the sample from outside chamber to inside. Sometimes it is necessary to prepare the samples before using (cleaning by acetic acid, alcohols and distilled water followed by nitrogen blow to remove the dust particles).

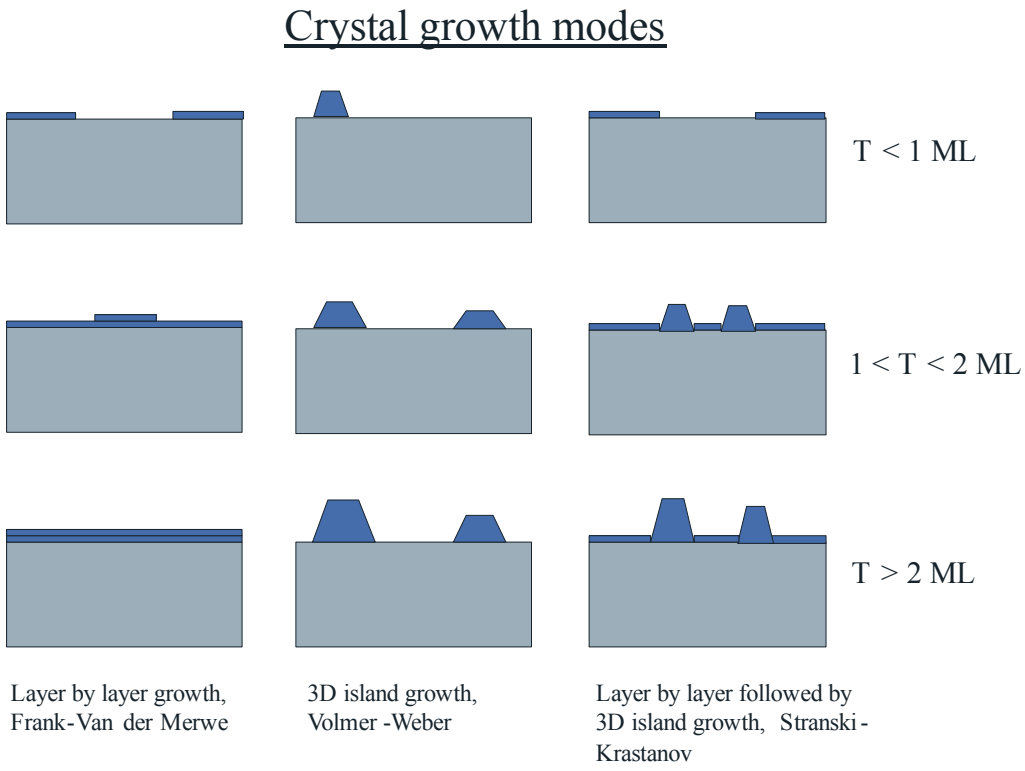


Figure 4.9: Crystal growth profile, showing different type of growth mechanism. Θ or T signifies surface coverage factor

The major interest of this process is to check for growth geometry as it would be interesting to see how the molecular channels are formed inside the trenches as they determine the electrical conductivity of the system. Also, as the growth is supposed to be crystalline, the number of grain boundaries will determine the conductivity and also the spin transport mechanism. The samples are broken and SEM technique is applied to check for the trench fill ups.

Growth nature: The thin film growth can be of 3 types,

(a) Layer by layer growth (Frank-van der Merwe type). This is 2-dimensional growth. The adatoms attach to the surface resulting in atomically smooth and fully formed layers. So, adatoms use to wet the surface completely. Epitaxial growth typically follows this pattern.
(b) Growth by island formation (i.e. nucleation, Volmer-Weber type). In this type, 3-dimenasional islands are formed and they gradually grow up. So, the film adatoms does not completely wet the surface, the contact angle being 0 < Theta < 180.
(c) Growth by both layer and island formation (Stranski-Krastanov type). This incorporates both types discussed before [17].

The growth mechanism depends firmly on surface energy parameter.

y_s : surface energy of the substrate (i.e. upper metal surface).
y_f : surface energy of the film (i.e. 'CuPc' film).
y_{sf} : interface energy of the substrate and the film.

So, for FM growth mode, $y_s > y_f + y_{sf}$, for VW growth mode $y_s < y_f + y_{sf}$, and for SK growth as well, $y_s > y_f + y_{sf}$ with crystal misfit. For FM growth mode, surface adhesive force is stronger than adatomic cohesive force and for VW growth mode, opposite thing happens.

The organic molecules are deposited and discussed in later sections.

5. Measurements and characterization

This chapter takes care of the measurement values taken at different stages of process flow, instruments behind this (note that different processes are used for different wafers intentionally), SEM imaging at different stages of the process, characterization and the final results. This chapter is divided in different sections for a proper approach to discuss. The parameters are changed continuously, majorly based on microscopic images taken at different instances of the process flow. The results at different stages of the processes are also discussed and analyzed, so that a proper understanding is developed about this part of the project. As already mentioned, the experiments started with 10 set of wafers and further 10 was used later.

5.1 Lithographic mask measurement

Trench isolation of the lithographic mask is measured and noted down. This step is done to make sure that proper dimensions are transferred into the wafers as per design. All the readings are tabulated for two different geometries. All units are in nm.

Trench dimensions (‘type 1’ geometry):

	1	2	3	4
A	854	851	857	855
B	853	863	860	858
C	903	895	916	906
D	910	893	909	893
E	952	942	958	958
F	952	944	944	958
G	953	955	956	957
H	994	996	998	978
I	986	995	994	993
J	1050	1059	1054	1048
L	1045	1061	1050	1061

Trench dimensions (‘type 2’ geometry):

	5	6	7	8
A	862	862	860	844
B	839	839	838	846
C	912	914	915	902
D	912	900	915	900
E	961	960	944	947
F	971	948	947	935
G	956	940	940	935
H	991	978	986	968
I	990	990	985	983
J	1059	1057	1051	1029
L	1055	1043	1028	1043

Table (iii): These two tables note down actual trench geometry transferred onto the wafer

It is noted that the observed data varies a little with the actual theoretical data but that should not be a serious problem for the upcoming steps. 'Leitz Ergoplan' (fully monitored and optionally software controlled) high performance microscope is used for this measurement.

5.2 Visual inspection:

This step is done by optical microscope. It is observed that the pattern has been transferred properly with good dimension. A figure is also provided to show how the structures look like under the microscope.

5.3 Anisotropic etching measurement:

This step signifies how much oxide is being removed during the anisotropic plasma etching step for the mask restructuring. 'DEKTAK' machine is used for the measurement purpose. 'DEKTAK' is a typical profilometer to measure the step heights, trench depths. This is a surface contact measurement technique using a very low force stylus, being dragged across a surface. There will be a certain display range of data. The vertical resolution is quite small and the lateral resolution would be limited by the tip geometry. The software can display data in the PC.

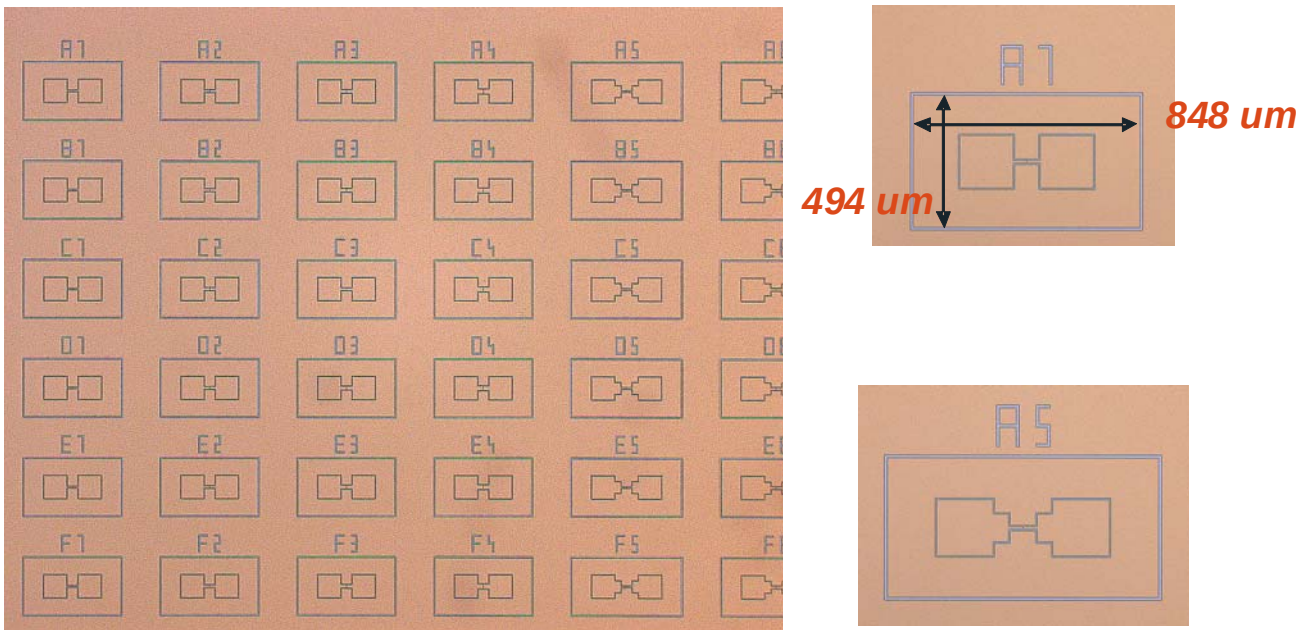


Figure 5.1: Lithographic images taken by optical microscope

Thickness measurement of oxide after anisotropic plasma etching (measured near test fields):

	wafer 1	Wafer 2	wafer 3	wafer 4	Wafer 5
Position TF2	496,2	497	484,8	493,7	476,9
Position TF3	498	499	492	494,6	480,4

Table (iv): This table notes down the oxide thickness after anisotropic plasma etching

Optical microscopic image is also taken. Lithographic and this image look similar.

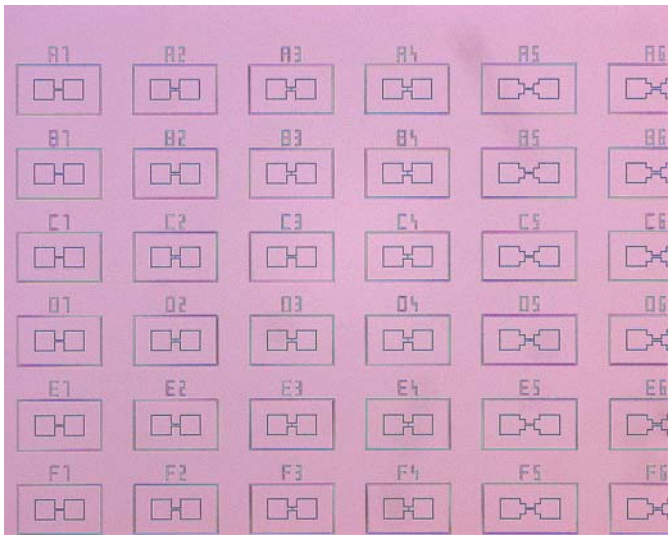


Figure 5.2: Image taken after anisotropic etching

5.4 DRIE measurement

Some wafers were etched by 3 um deep, some by 6 um, 9 um and 5 um. The depths of the trenches were measured by 'DEKTAK' again.

The measurement values are listed below.

	wafer 1 (3 um)	Wafer 2 (3 um)	wafer 3 (6 um)	wafer 4 (6 um)	Wafer 5 (5 um)
Position TF1	3,493	3,6018	6,4258	6,6837	9,63424
Position TF2	3,1762	3,3362	6,0556	6,1963	8,8897
Position TF3	3,58816	3,6725	6,684	6,7333	9,74367

Table (v): This table jots down DRIE etch depth parameters

The test fields 1, 3 were at the middle of the wafer (ref: wafer grid of Appendix) and hence etching rate is higher for them whereas the test field 2 is at one side of the wafer where etching rate is slower. This describes the deviation in the values. Also, in the same position, depth is little higher than what expected, but this would not affect the results much.

Typical SEM image profile is also provided. It shows that DRIE introduces scallops and rough edges into the sidewalls of the structure. The formation of scallops might influence the oxide and metal deposition characteristics and later the formed organic molecular channel. Also, the trench width reduces somewhat over depth. It also seems that the etching is well anisotropic one.

5.5 PECVD measurement:

By PECVD, a further around 200 nm thermal oxide (particularly for sidewall passivation, as discussed earlier) is deposited. This adds up with the oxide mask (500 nm) to make the top oxide surface around 700 nm thick. Oxide thickness at the surface is measured. This process is important as one needs to decide on the etching time for the next step. If the deposition is higher, then the etching time should be kept higher. TF signifies the test fields. It is seen that the data are almost near 700 nm range, and very close to each other. They are actually a little less than that but this is not a big problem for this process. 'DEKTAK' is used again as the profilometer.

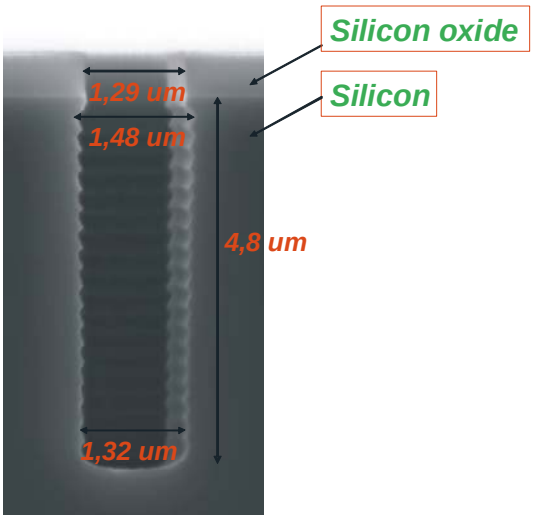


Figure 5.3: Image showing DRIE step and scallops are visible clearly near the trench walls. All the necessary dimensions are noted. It is noticed that the trench width increases just beneath the mask and this value then decreases somewhat with depth of the trench. This trench was to be etched by 5 um.

Thickness measurement of oxide after PECVD (nm) is shown.

Wafer	1	2	3	4	5	8	9	10
TF1	681,8	682,03	673,31	685,09	683,96	681,04	683,99	678,91
TF2	684	682,95	678,33	679,9	688,7	685,9	684,9	687,28
TF3	681,16	683,24	670,42	677,46	664,02	681,45	681,85	679,83

Table (vi): This table notes down the oxide thickness after PECVD

These values are taken for first experimental set and first 10 set of wafers. 6th and 7th wafers were used for other purposes. So, the data are in accordance of what is desired.

5.6 Spacer etching measurement:

Again, the oxide thickness at the top of the wafer is measured. This value should be lower than 500 nm as the aim was to etch away the complete oxide from the bottom of the trenches (hence etch away the same amount of oxide from the top as well), which makes sure that silicon (not anymore oxide) rests at the bottom. As the next step would be isotropic silicon etching at the bottom (hoping that no oxide layer stays at the trench bottom), this step plays a crucial role.

Thickness measurement of oxide after Spacer etching (nm):

Wafer	1	2	3	4	5	8	9	10
TF1	403,3	382,48	424,38	500,25	412,92	452,3	451,33	420,86
ground	0	7,34	8,59	0	4,73			
TF2	467,95	444,53	510,8	446,68	500,07	482,66	479,54	476,25
ground	0	14,22	9,18	11,25	15,43			
TF3	449,11	425,62	483,2	425	471,98	448,39	444,68	420,26
ground	0	0	0,74	10,98	0			

Table (vii): This table notes down the oxide thickness after spacer etch

The deviations in values for different test fields occur for the same reason discussed before. Etch rate is sensitive to the position of the test fields in the wafer. In some of the places, the oxide thickness is quite lower than expected (500 nm) but it is not a big problem as this oxide would be etched away in the next steps and deposit fresh oxide layer again by LPCVD or Thermal oxidation. 6^{th} and 7^{th} wafers were kept for other purposes.

5.7 Isotropic etching measurement:

When some of the wafers were broken (particularly in coming sections), SEM images were analyzed. One of the samples (wafer 1, undergoing TO, the structure is 'F3') showed horizontal (isotropic) etch width as 3,2 um and vertical as 2,3 um. So, the degree of anisotropy would be A = |1-(3,2/2,3)| = 0,39.

5.8 Naked silicon trench measurement:

The optical microscope is used once again to measure for trench dimensions (like last case) but the values do not seem to differ much. For this reason, a SEM image would be a far better option. SEM images of any structure would be quite helpful as on basis of these images, a decision has to be taken on how much oxide (followed by metallization) should be deposited. Each and every time in this project, the same treatment is carried out for different wafer sets. Once again all these values are tabulated here. All dimensions are in um. All data are the result of top SEM imaging of the different structures. It is seen that 'A1' and 'A5' would give almost same values as for obvious reason. This data corresponds to one of the wafers.

A1	B1	C1	D1	E1	F1	G1	H1	I1	J1	L1	A5
1,224	1,213	1,288	1,284	1,295	1,31	1,31	1,36	1,37	1,444	1,407	1,277

Table (viii): This table notes down the Silicon trench opening (top view of naked Silicon, dimensions are in um)

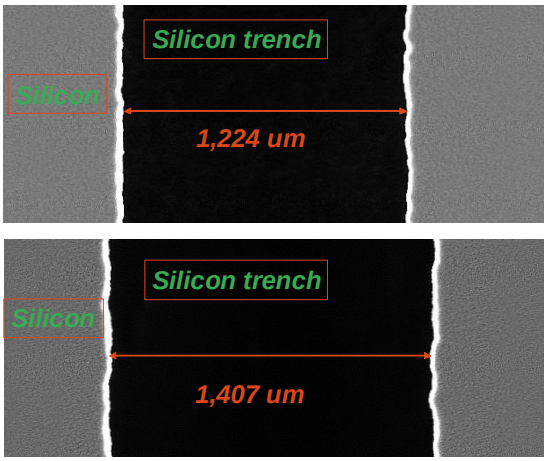


Figure 5.4: The image shows the TOP SEM view of the naked Silicon trenches. First one is for 'A1' (800 nm trench width as per design) and the second one for 'L1' (1000 nm) structure. It seems that the trench opening is little higher than designed. The trench edges are shiny.

This data is for another wafer, being undergone same technology steps. Units are in um.

A1	B1	C1	D1	E1	F1	G1	H1	I1	J1	L1
1,377	1,15	1,139	1,183	1,21	1,288	1,295	1,291	1,332	1,325	1,381

Table (ix): This table jots down the Silicon trench opening of another wafer

The 'A1' trench data in the first column is a measurement fault.
Along with above mentioned wafers, the same data for new set of wafers are provided. As this dimension is significant for next technological steps, values are tabulated.

A1	B1	C1	D1	E1	F1	G1	H1	I1	J1	L1
1,213	1,213	1,288	1,284	1,329	1,329	1,321	1,377	1,366	1,433	1,414

Table (x): This table jots down the Silicon trench opening of yet another wafer

It is noted that the values are not exactly 800 nm to 1000 nm but higher. A reason behind this might be the occurrence of mask underetching. Also, the difference between the maximum and minimum values are (1,444 - 1,213 = 0,231) 231 nm and this is almost in accordance with the design (1000 nm - 800 nm = 200 nm). The images are taken for another set of the wafers (as tabulated) and the same things seem to happen. Also, the trench edges seem brighter for higher reflectivity.

5.9 Oxide profile characterization:

As there are two processes followed (and TO), both of them are discussed separately as their deposition profile would differ a lot.

5.9.1 LPCVD:

5.9.1.1 Oxide thickness measure:

In this step and for the first experimental results, 550 nm of oxide was deposited by LPCVD. As the minimum trench opening is around 1213 nm (for the first set of wafers as tabulated before), this decision was taken (as LPCVD profile was not known initially). This would contribute (theoretically) to a total amount of 1100 nm (from both sides) of oxide and hence the trench opening would be around 110 nm where the metal could be deposited (followed by organic molecule deposition). A close look at the deposition characteristics is provided in subsequent parts.

	Wafer 2	Wafer 4
position TF1	433,73	435,62
position TF2	444,39	445,82
position TF3	431,77	433,58

Table (xi): Table showing the trench opening near the TF surface after LPCVD

In one of the new wafers, 700 nm of oxide was deposited to keep the trench width more than 300 nm (the smallest trench width even after metal deposition). How much a higher channel width factor would influence the spin transport could be analyzed by this way (or when transport phenomena vanishes). The minimum trench was found to be 297 nm and the maximum 486,8 nm. For other wafers, as trench opening near the surface seemed to be higher (ref. first experimental results), 800 nm of oxide is deposited. The minimum and maximum trench opening was noted.

SEM profiles are depicted below. Every detail of the images is mentioned with the corresponding images.

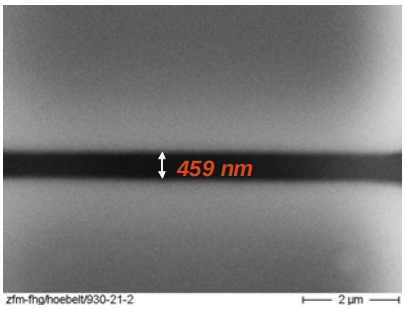


Figure 5.5: Typical top SEM view of 'A1' (1224 nm naked Silicon trenches) structure after 550 nm of oxide deposition by LPCVD. From the top view, the structure geometry is never revealed.

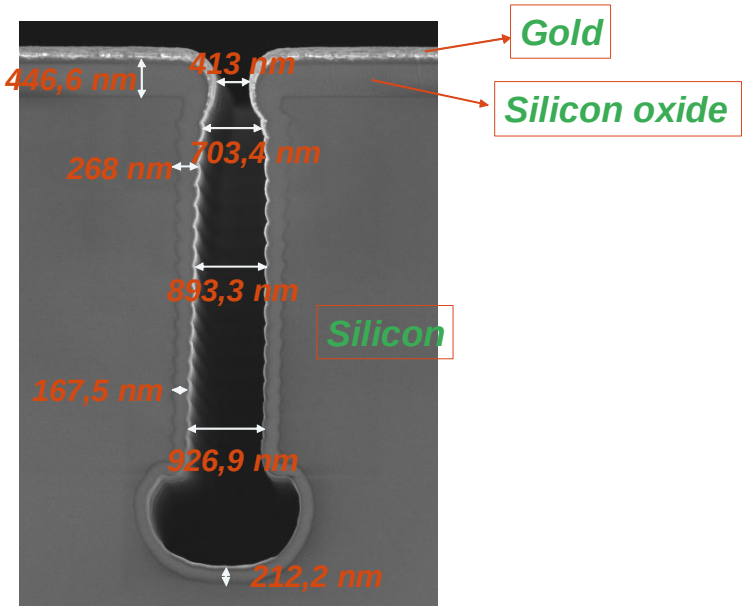


Figure 5.6: Typical LPCVD profile (550 nm of oxide deposited on the top followed by 100 nm Gold sputtered). This was 'A7' (naked Silicon trench opening below 1200 nm) structure. All the necessary dimensions are listed. The picture is little bit tilted but the dimensions could be taken as more or less perfect. LPCVD shows a very different profile than thermal oxidation, the thickness of oxide varies significantly with the trench depth. The trench opening increases over trench depth and it is minimum near the surface. The scallops are present near the Silicon – Silicon dioxide interface region and in the trench walls, still Silicon and the oxide parts are clearly distinguishable. The trench bottom is not that flatter compared to thermal oxide profile. Deposited Gold as usual seems quite shiny, its thickness decreases gradually with depth as well. Gold does not seem to create a short circuit at the trench bottom.

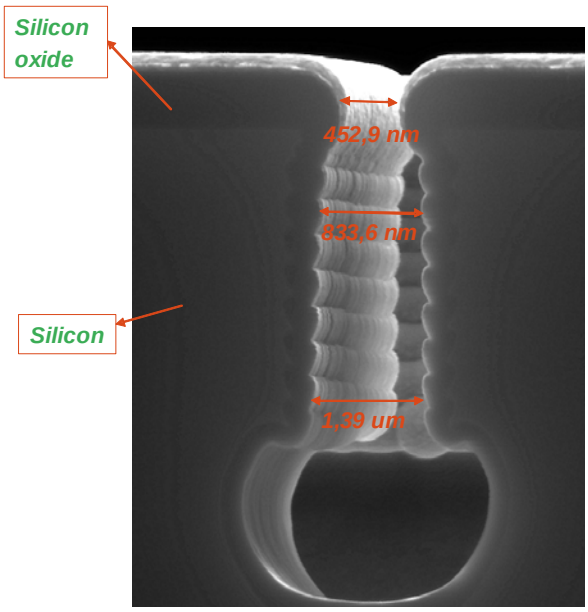


Figure 5.7: Another LPCVD profile (550 nm of oxide deposited on the top followed by 100 nm Gold sputtered). This was B8 structure (naked Silicon trench opening 1213 nm). Important dimensions are mentioned (although the structure is little tilted)

5.9.1.2 Cross section SEM image analysis:

Top SEM image was taken for first experimental wafers; it revealed that the trench opening for the A1 geometry was 459 nm, which seems higher.

For a better electron microscopic imaging, some wafers were broken into small chips in such a way that some of the structures are met. This SEM images is taken to provide a cross sectional view of the structures as only a top view may not be enough to reveal the oxide deposition characteristics. The images are provided and discussed.

It is seen that if someone deposits some amount of oxide at the top of a trench by LPCVD, the typical sidewall deposition would be much less, hence making the deposition characteristics across a trench quite unconformal. Some data are analyzed and noted down. One of the structures shows that for 450 nm oxide deposition at the top surface, the immediate side walls grow 270 nm each (an approximation is done as due to presence of scallops discussed earlier). Again, a 590 nm of deposition at the top contributes to around 300 nm of sidewall coverage (infact, the oxide thickness lowers while someone goes down to depth). On average, this bears a 1,75:1 ratio of top to immediate side wall oxide deposition characteristics. Also, due to presence of scallops, thickness across the trench varies a lot.

5.9.2 Thermal oxidation:

As the first decision was to deposit 550 nm of oxide from both sides (LPCVD), same has to be calculated for the thermal oxidation as well. As it was discussed before, only around 54 % of oxide stays above the surface level (this happens due to the diffusion property of oxide, this 54 % is equivalent to 550 nm), (550/0,54) = 1018,5 nm of oxide should be deposited for the same equivalence. First decision would be to deposit 1000 nm. Also, top deposition and side wall deposition characteristics would vary. It will be shown in the proceeding parts; a SEM image reveals the trench opening near the surface is much higher. For this reason, 1050 nm of oxide was deposited in the next experiment. In these two cases, the outcome would differ and this would be discussed.

5.9.2.1 Top view:

Top view (SEM image) of the structures after 1000 nm of TO deposition is shown.

A1	B1	C1	D1	E1	F1	G1	H1	I1	J1	L1	A5
111,7	113,9	169,7	169,7	169,7	174,2	205,4	241,2	250,1	317,1	303,7	158,5

Table (xii): Table showing the trench opening after TO by 1000 nm, all dimensions are in nm.

So, the minimum opening is 111,7 nm and maximum is 303,7 nm. They bear a difference of 192 nm. Again, for the ‘A1’ structure, the trench opening was 1,224 um before oxidation (i.e. naked ‘Si’ trenches) and 0,1117 um after thermal oxidation, so this gives rise to 1,112 um difference but 1 um oxide was deposited. For ‘B1’ structure, this is around 1,1 um , for ‘C1’ structure, it is 1,118 um and for ‘D1’ structure, it is 1,114 um and so on. These data signifies that from the top view of SEM, it is not possible to detect the exact point where minimum trench opening happens to be and TO profile is different than LPCVD one. Again, the edges

would look brighter and a number of bright lines are noticed in the image. This makes it obvious that the trenches covered with oxide contains many edges.

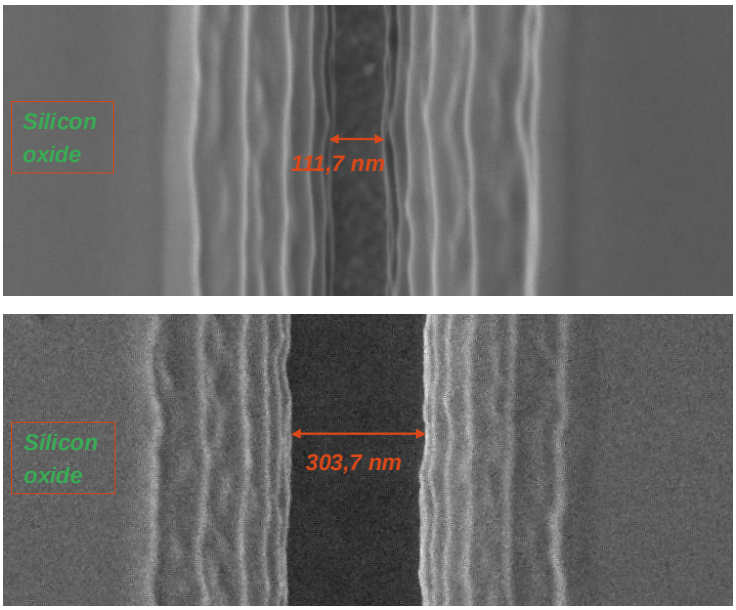


Figure 5.8: These two images show top view of 'A1' (1224 nm naked Silicon trench) and 'L1' (1407 nm naked Silicon trench) trenches after TO deposition of 1000 nm. Presence of a lot of (shiny) edges with minimum trench opening of shown dimension is clear but a proper conclusion about the trench geometry can not be drawn.

In the second set of experiments, 1050 nm oxide is deposited but it seems the trenches with lower opening (like A1 or B1 etc) are closed.

5.9.2.2 Cross sectional view:

Some wafers are broken to have a side view SEM image for better understanding. The profile is completely different than LPCVD one.

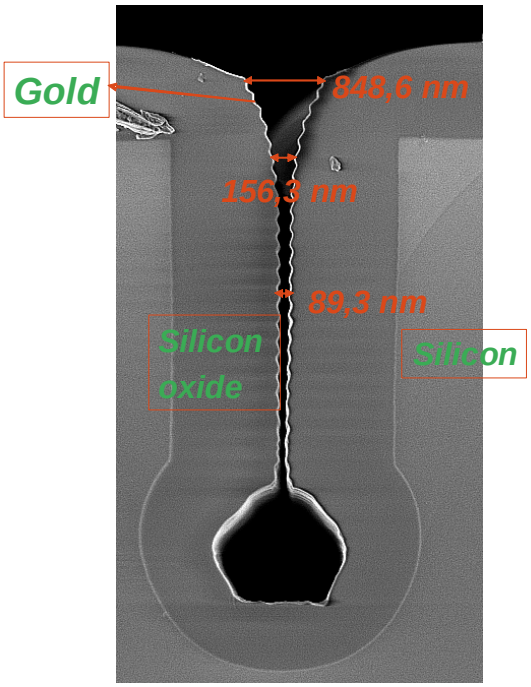


Figure 5.9: Thermal oxidation profile, 1050 nm oxide is deposited followed by a sputter of 10 nm of 'Au + Cr'. 'F8' Structure (1288 nm wide naked Silicon trench) has been shown. The image is somewhat tilted but dimensions are ± 10% accurate. The trench opening gradually decreases with depth and it seems like there is no short circuit of oxide (or metal). Trench bottom is comparatively flatter. The silicon and silicon dioxide portions are distinguishable, the deposited Gold seems brighter. As this is F8 structure and trench is almost closed at the bottom, it seems the trenches are completely filled at least for small width Structures (like 'A', 'B' etc).

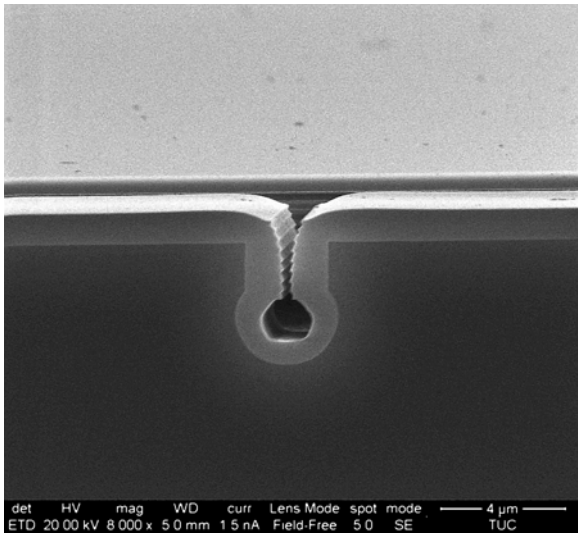


Figure 5.10: Thermal oxidation profile, the structure Shown is 'F3'. Deep etching of Silicon followed by isotropic etching are clearly visible. The structure is clear and the Silicon and Silicon dioxide are distinctly visible. Gold is at the top of the surface. Scallops are present in the trench walls.

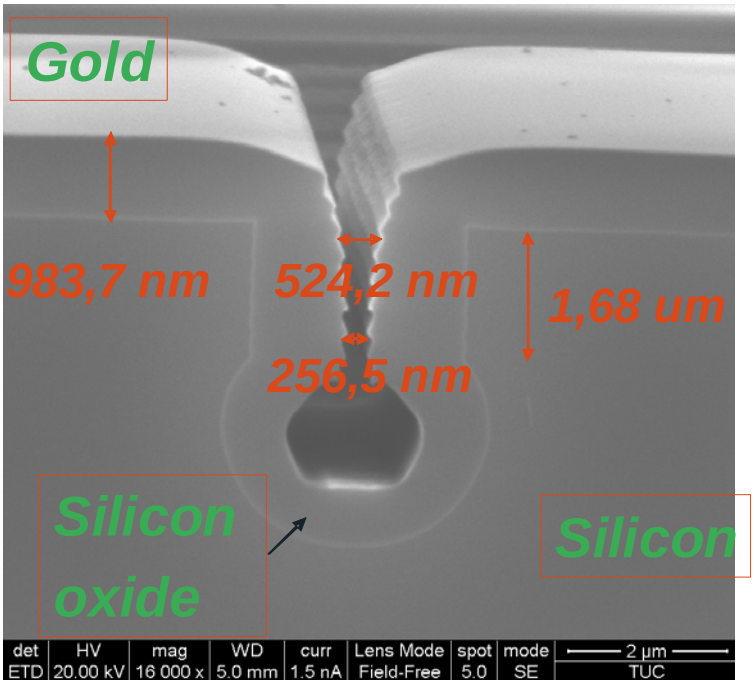


Figure 5.11: Thermal oxidation profile, 1000 nm oxide is deposited followed by a sputter of 40 nm of 'Au'. 'H4' Structure (1360 nm wide naked Silicon trench) has been shown. This image is also tilted but dimensions are ± 10% accurate. The trench opening gradually decreases with depth and it seems like there is no short circuit of oxide (or metal). Trench bottom is flatter.

5.9.3 Comparison between Thermal deposition and LPCVD:

Here, a series of comparison is made between these two technologies.

1. In LPCVD profile, the trench opening increases with depth but for TO, the deeper trench goes, the thinner it is.

2. Near surface, TO trench opening is much higher, although almost same effective amount of oxide was deposited in both of the LPCVD and TO methods.

3. Good edge coverage with a positive sidewall angle for TO results in an effective device according to the whole trench height.

4. Bad edge coverage for LPCVD results in an effective device at the top edge of the trench.

5. Scallops in the silicon are clearly visible in LPCVD profile (Si and the Silicon dioxide interface region) whereas in TO profile, this is completely absent. This happens as the oxide diffuses into silicon surface during TO. In fact, these images prove the idea itself.

6. The structure profile at the trench bottom (isotropically etched part) is different for TO and LPCVD.

7. The amount of oxide deposited at the top surface and the side walls of the trenches does not vary much for TO but varies significantly for LPCVD profile.

A significant thing is that if someone has to make the organic molecule channel length less than 100 nm (or even 200 nm) near the surface zone of the trenches, the TO profile would completely fill up the trenches even just below 1 um deep (ref: the SEM images of TO). This phenomenon in turn will make sure that a further metallization would cause short circuit of the electrodes and the idea of isotropic etching will be of no use. To analyze spin transport, one is not allowed to go beyond 300 to 400 nm transport channel length and hence LPCVD should be favoured.

5.10 Electrode measurement:

In all of the wafers (for the first experiments), 'Au' is used as metallization medium. 40 nm of Gold is deposited on the top (of the wafers for whom 1 um TO was deposited). Sputtering method is used as mentioned before. In the other wafer (where 1050 nm of oxide was deposited), 10 nm of 'Au + Cr' were deposited. These values were decided on the basis of how much open space was there for metal deposition and keeping another constraint in mind that a molecular transport channel of around 60 nm range (minimum) could be formed near the surface region of the trenches. The below pictures show SEM profile of typical structures. It is again noticed that the deposition is not uniform, the deposition thickness gradually reduces with trench depth. This deposition characteristics is also very significant like previous cases, as this would influence the organic channel which is going to be formed. Gold has a high atomic number, and coating with gold produces high topographic contrast and resolution. Also, silicon, oxide and gold can be distinguished in some of the SEM images (gold show high reflectivity). Film purity would be enhanced by a clean sputter target and clean process gas.

Top view SEM images are taken for the structures having 1050 nm of TO followed by 10 nm of 'Au + Cr'. It seemed that some of the structures are fully filled and maximum trench opening noted to be 113,9 nm.

A short note on the cross sectional view of the structures is also provided. It is noticed that to deposit 115,8 nm of gold at the top surface, around 59 nm of gold is grown up at the immediate sidewalls. In another structure, a 98 nm of gold deposited at the top surface gives rise to 58 nm gold deposition at the immediate sidewall surface. On approximation, it can be considered that a 1,9:1 ratio of top to immediate side wall gold deposition is a good choice. Gold thickness becomes much less even after 1 um. The deposited gold does not seem to have any short circuit from simple inspection.

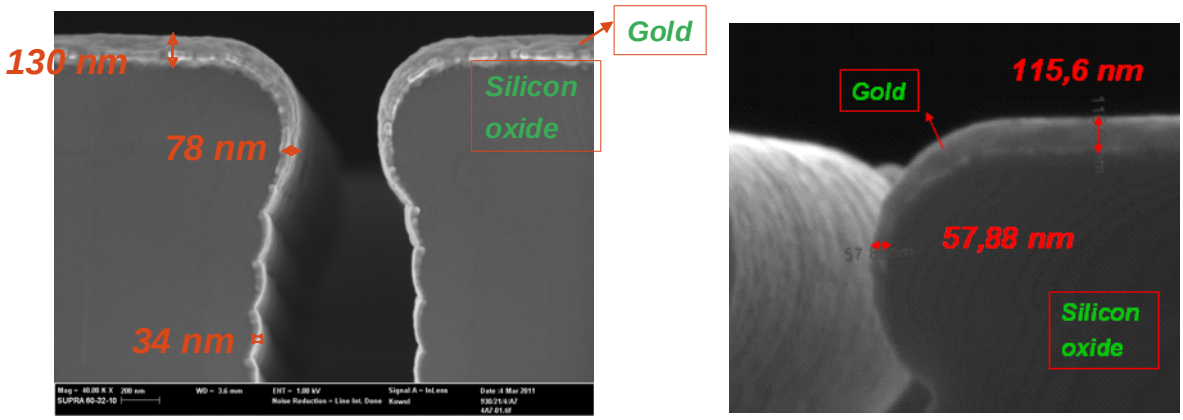


Figure 5.12: Deposited Gold profile on two of the structures. It is noted down that Gold Deposition characteristics, like LPCVD, varies significantly. Gold thickness diminishes with depth of the trench, as mentioned earlier. The important dimensions are also noted down.

For the new set of wafers, 100 nm Cobalt sputtering is used in some of them. Top SEM image reveals the trench opening and they are listed below. They do not seem to be short circuited.

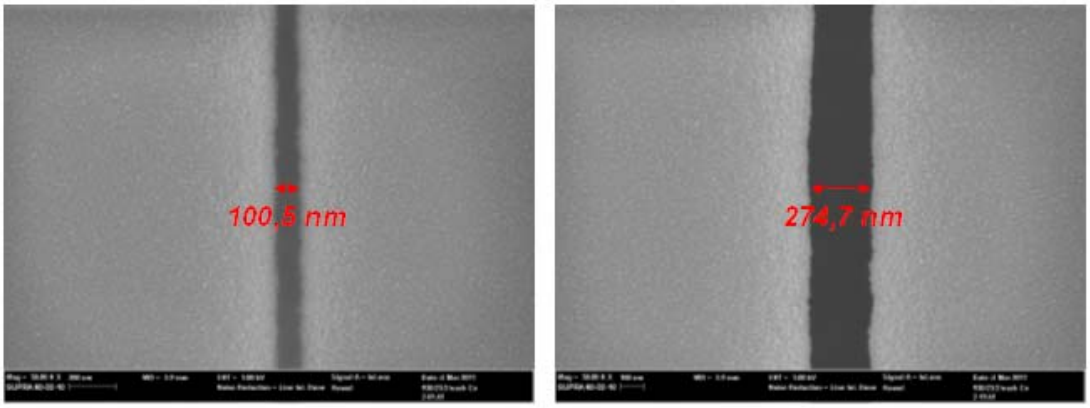


Figure 5.13: Image showing highest and lowest trenches.

Top view after 100 nm Cobalt sputter (units are in nm):

A1	B1	C1	D1	E1	F1	G1	H1	I1	J1	L1
100,5	98,25	151,8	145,1	187,6	174,2	178,6	207,7	205,4	274,7	252,3

Table (xiii): Table showing the trench opening after 100 nm Cobalt sputtering

The difference between two extreme structures (in terms of width) is noted to be 174,2 nm and this value is in accordance to the expectation. The minimum and maximum trench width seemed to be proper.
For some of the wafers, 100 nm Gold is deposited and noted down as well.

Top view after 100 nm ‘Au’ sputter (units are in nm):

A1	B1	C1	D1	E1	F1	G1	H1	I1	J1	L1
105	98,25	109,4	145,1	183,1	192	178,6	221,1	218,8	276,9	256,8

Table (xiv): Table showing the trench opening after 100 nm Cobalt sputtering for another wafer

The data seem to be good, any presence of short circuit seem to be absent.

5.11 Thin film electrical parameters measurement:

To check for the small trenches, whether the deposited metal short circuits them or not, resistance measurement would be a good option. Also, capacitance measurement can be useful. Resistance value would differ for a short circuited metal deposition and for an open circuited structure. Now, if the resistance measurement data shows an open circuit, there might be two possibilities,

(i) The metal does not fill up the trenches at all (but the metal film is not continuous near the trench opening).
(ii) The metal fills up a portion of the trenches, and the deposition inside the trench is discontinuous.

Now, this thing will also depend on the amount of the metal deposited. If the measurement data shows short circuit, then also there will be several possibilities,

(i) The metal deposition is continuous and it fills up properly the trenches (i.e., the metal fills up the bottom of the trenches including the isotropically etched part).
(ii) The metal deposition is continuous and it fills up some part of the deep trenches (i.e. the metal does not fill up the isotropically etched part).
(iii) The metal deposition is continuous at the substrate surface and it does not fill up the trenches at all.

All these facts will depend on how much metal is deposited and the growth nature and dynamics.

During capacitance measurement, the results will be much different as there are too many stray capacitance effects. A calculation on the possible capacitance values is performed. Now, if the resistance measurement data shows open circuit, then only capacitance measurement is relevant.

5.11.1 Resistance measurement:

Resistance measurement can be of different types like two probe or four probe resistance measurement. 4 probe measurement method uses separate circuits for current measurement and voltage measurement whereas 2 probe system is the simplest one, using only one circuit to measure current and voltage. 4 probe measurement technique is more perfect as it omits wiring and contact resistances from the final result. It is enough to perform a 2 probe measurement to check if a circuit is open or short.

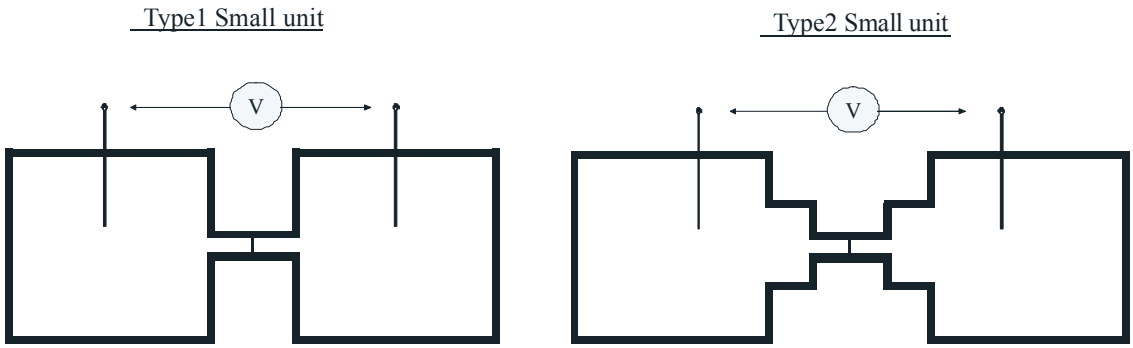


Figure 5.14: These images show the electrical contacts and applied voltage

While resistance measurement, one very important thing is how much voltage could be allowed to act on the organic molecules. Also, the structure resistance would depend on the measurement system, precisely the position of the tip on the sample. It is assumed that the resistance would lie in between megaohm to gigaohm range. So, a lower applied voltage (typically around 10 V) would give rise to a nA to uA range current which could be measured easily.

The reason behind measuring the electrical resistance of the thin films before studying the magnetoresistance behaviour is very obvious that someone would like to test whether the charge transport is occurring at all before going for a time consuming magnetoresistance study.

The first experimental set of wafers showed open circuit characteristic of the resistance (wafers with only metal deposited, not organic molecules). Another set of resistance measurement is done after OMBD (discussed later) and the results are shown in this chapter.

The problem in measuring the resistance of this type of thin films is also obvious. To reach the metallic contacts by the measuring tips, one needs to scratch (with a scalpel) the organic molecular layer very precisely (as the organic molecules are deposited all thoughout the sample, not specifically near the trenches). In reality, this operation was only possible for some samples but not all. In some of the samples, only 10 nm of Gold is deposited, so this is even tougher for them. If the electrical and magnetoresistance experiments seem to be difficult, one has to think about selective deposition by using further masking.

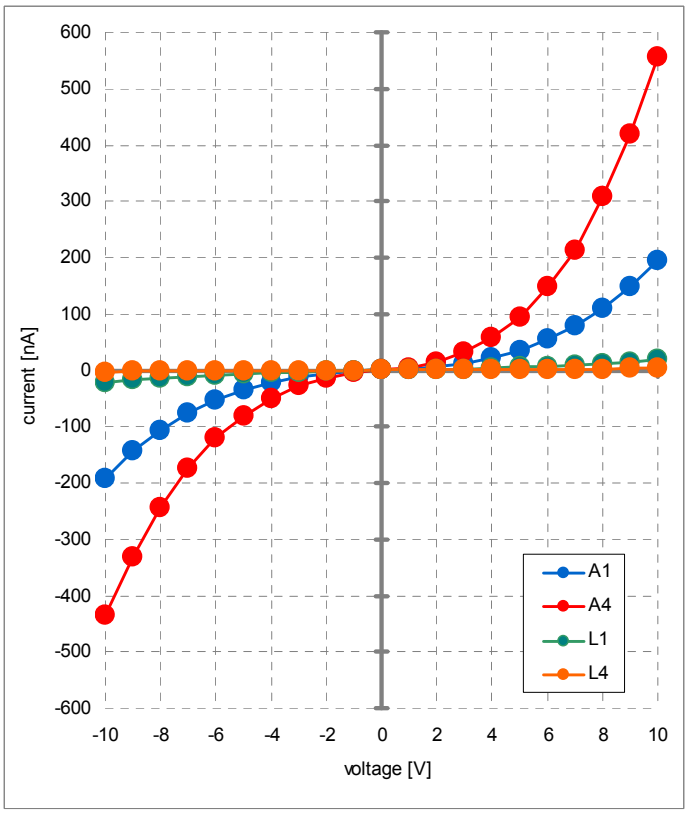


Figure 5.15: Typical I-V characteristics of the sample (LPCVD profile). This is with 100 nm Cobalt deposited at the top, 200 nm 'CuPc'. The curve is nonlinear in nature but this can be explained like if someone would increase the voltage, contact resistances gradually become a dominating factor. The resistance is in giga ohm range. Different structures ('A1', 'A4', 'L1', 'L4' etc) show different characteristics as their geometric parameters vary as discussed earlier. The 'A' structures would show lesser resistance than 'L' structures as for them the channel length is lower. The '1' structures would show lesser current than '4' structures as for '4' structures, the cross sectional area is higher making the channel resistance comparatively lower; thus making current higher. So, this curve shows the resistance data of the thin film 'CuPc' (sandwiched between Cobalt electrodes) under the absence of any external magnetic field.

Data analysis and discussion:

1. That graph shows some significant values which are mainly noted down.

	A1	A4	L1	L4
R (±1V) [GΩ]	0,481	0,205	1,53	10,56
R (±10V) [GΩ]	0,052	0,020	0,50	3,10

Table (xv): Table showing the resistance data of different structures based on (nonlinear) I-V characteristics

So, the resistance value varies a lot. One can calculate resistivity of the film by using the formula $R = \rho.(l/A)$, so $\rho = R.(A/l) = 481.(40.1)/100.10^{-3} = 192400$ MOhm-um.

2. As mentioned earlier, contact resistances influence the characteristics. Contact resistance include,

- used needle to metal contact for both sides,
- metal to the organic molecules contact from both sides.

The resistance shown would be sum of contact resistances, resistance of the organic molecules and somewhat resistance of the metal as well.

5.11.2 Capacitance measurement:

The major capacitance will be formed between two trenches, along with other stray capacitances, formed between metal and the silicon (due to presence of the insulating oxide).

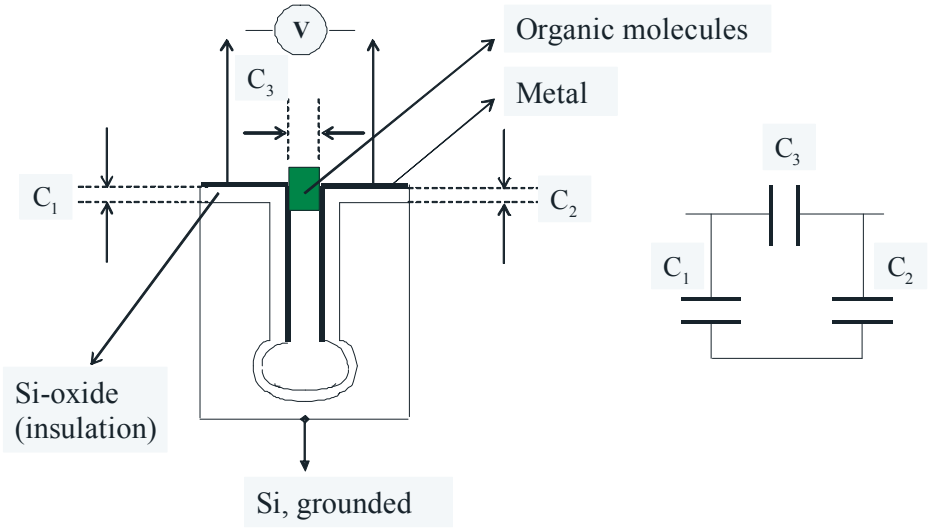


Figure 5.16: Image showing how the capacitors are formed near the trench

Mathematical calculations:

Say, 'A4' structure is taken.
$\varepsilon_{oxide} = 4$ is assumed.
For this structure, deposited gold at the top = 10 nm. Gold thickness near the trench opening in the sidewalls = 5 nm.
Oxide thickness (Thermal oxidation) = 1050 nm.
A final airgap near the trench = 40 nm is assumed (when the trenches are not filled up at all).

Calculation for C_1 and C_2:

A = cross sectional area or overlapping area

$$= (200\ \mu m).(200\ \mu m) + (40\ \mu m).(50\ \mu m) - 42000\ \mu m^2$$

So,

$$C_1 = \frac{\epsilon_0 . \epsilon_{oxide} . A}{d_{oxide}}$$

Where $\varepsilon_0 = 8{,}85.10^{-12}$ F/m, $\varepsilon_{oxide} = 4$, $d_{oxide} = 1050$ nm.

So, $C_1 = 0{,}1416$ pF = 141,6 fF.

Also, $C_2 = C_1$.

Calculation for C_3:

The metal is assumed to fill up the trench by, say, 'd' nm deep with the thickness 5 nm.

A_1 = cross sectional area or overlapping area =

$$(40\ \mu m).(d\ nm) - 0{,}04.d\ \mu m^2 - 0{,}04.10^{-3} m.(d\ nm)$$

$$C_3 = \frac{\epsilon_0 . A_1}{d_{air}}$$

So,

$$C_3 = \frac{0{,}354 d}{d_{air}}\ fF$$

where 'd' and 'd_{air}' are in nm.

Now, if d = 1000 nm, d_{air} = 40 nm.

$C_3 = 8{,}85$ fF.

Now, let us consider that the organic molecules fill up 1 um depth of trenches. This is a fair assumption as one would be concerned not about the actual capacitances but approximated range. In such a case,

A'_1 = new cross sectional area (or overlapping area)

$$= (40\ \mu m).(1\ \mu m) = 40\ \mu m^2$$

Now, $d_{CuPc} = 100$ nm approx.

$\varepsilon_{CuPc} = 4$ considered. Properties of CuPc are discussed in the Appendix.

Then $C_3' = \frac{8{,}85.10^{-12} A.40.10^{-12}}{100.10^{-9}}\ F = 14{,}16$ fF

So, it is noted that the parasitic effects are much dominating for the capacitance values.

5.12 Coating characterization:

As project's interest includes whether the organic material can fill up the trenches or not (if yes, then how deep can it enter and its profile), the trenches are coated by spin coating method and spray coating method, before using organic molecule deposition (couple of wafers are taken and coating treatment is done). Afterwards, the wafers are broken and SEM images are taken for both. A comparison can be made between these two methods.
During spin coating method, the photoresist is placed on the surface of the wafer, the wafer being set on a spin coater machine. The machine is made to rotate at a certain speed and the fluid spins off the edge of the substrate surface due to centrifugal reaction. The film deposition geometry would depend on the speed of rotation and surface of the substrate. The other film profile deciding factors are viscosity, drying rate, surface tension of the material to be deposited. The acceleration of the substrate towards the final spin speed can also affect the coated film properties. The film thickness would tend to decrease with an increase in spin speed and also the spin time. Another important fact is that high rpm promotes rapid drying of the resist solution and therefore it will not allow flow of the material into deep trenches. In this case, final thickness is kept 1,3 um, positive photoresist material OiR 906-12i series is used.

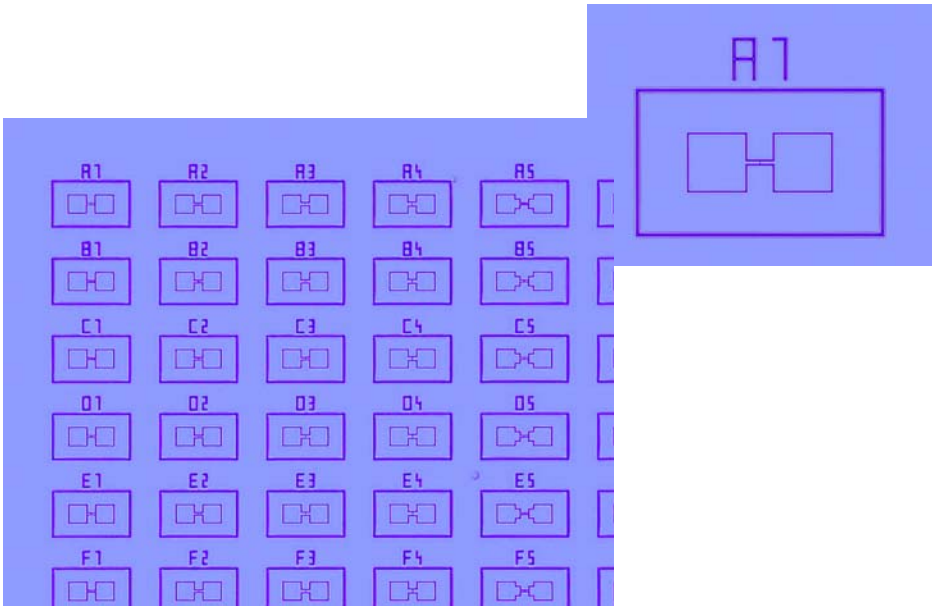


Figure 5.17: The images show the optical microscopic view of the wafer (with oxide and metal being deposited) after spin coating by photoresist material. The structures are clearly visible and all the present trenches are properly distinguishable.

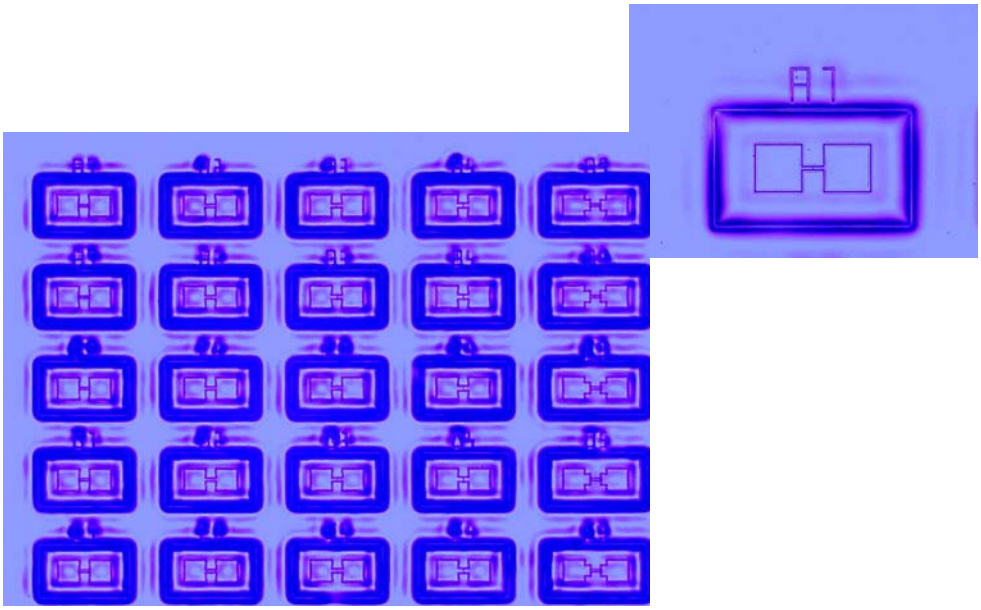


Figure 5.18: The images show the optical microscopic view of the wafer (with oxide and metal being deposited) after spray coating by photoresist material. The structures are visible but blurred somewhat.

For spray coating, sprayers are used. The resist is atomized into tiny droplets and this is made to move on the surface and millions of droplets form the growing resist film. Even 3 dimensional bodies can be spray coated. In the spray coating process, there is direct perpendicular impingement of the coating solution that promotes coverage into deep trenches. There are other types of coating techniques available like dip coating, roller coating (these are all variations of directly applying the coating solution across the topside of the substrate), meniscus coating (the substrate is inverted and passed over a laminar flow of coating material.

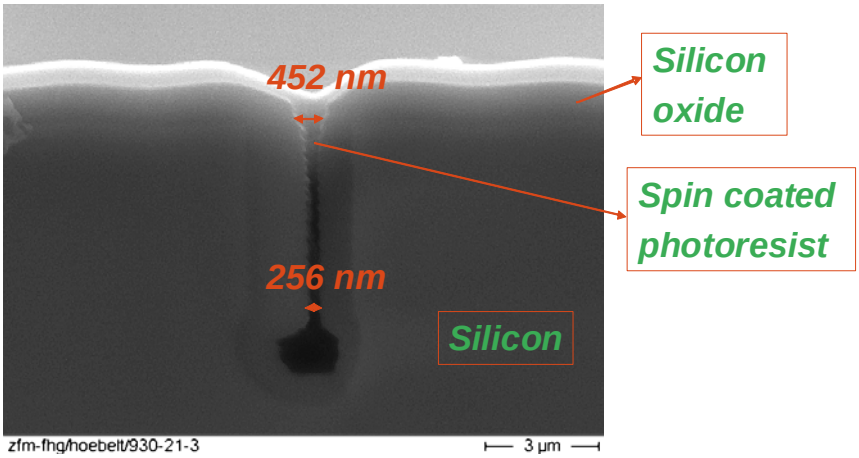


Figure 5.19: This image shows SEM cross sectional view of one of the structures being spin coated. The trench is clearly visible with the Silicon and the oxide (Thermal oxidation) part. The trenches are properly filled up by the resist, the image is not perfect due to the loading problem of SEM. Important dimensions are listed for this structure which are again ± 10% perfect. So, trenches with nanometer range opening can be filled up properly by spin coating method.

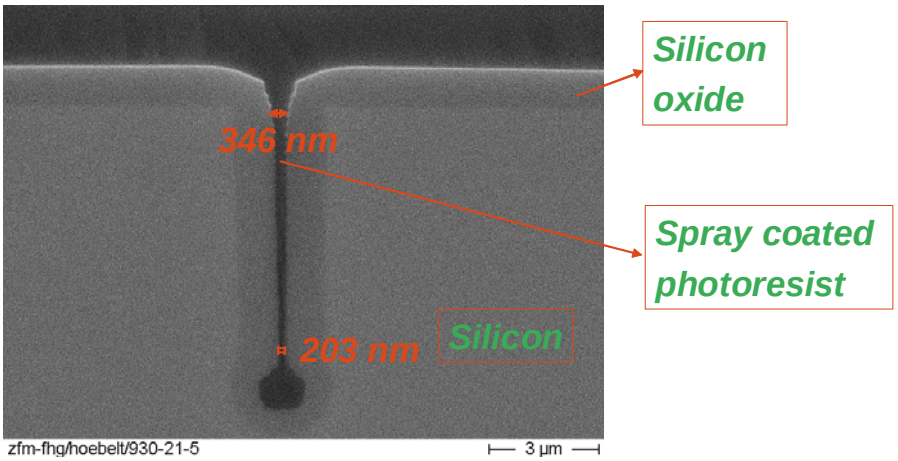


Figure 5.20: This image shows SEM cross sectional view of one of the structures being spray coated. The trench is clearly visible with the Silicon and the oxide part (Thermal oxidation). The trenches are properly filled up by the resist. Important dimensions are listed for this structure which are ± 10% perfect. So, trenches with nanometer range opening can be filled up properly by spray coating method as well.

The result is highly uniform coatings, even on substrates with relatively poor flatness), electrodeposited photoresist (this type of photoresist has typically only been used in the printed circuit board industry. Both positive and negative resist chemistries are possible) etc. Infact, sufficient flow of the coating material into high aspect ratio features depends on Coating method, coating solution etc. factors. In this case, AZ4999 photoresist material (transparent) is used. [18].

5.13 OMBD characterization

The samples and a part of OMBD process is discussed in this chapter rather than 'Fabrication' chapter. It is much easier to understand the steps here as one has better idea of depositions (oxide and metal) here at this stage of the report. The samples are prepared by 'CuPc' deposition on the top of the structures. Two structures are selected,

(i) Sample 1: with TO profile with 10 nm Gold on it.
(ii) Sample 2: with LPCVD profile and 100 nm Cobalt on it.

The organic molecules are not deposited on the wafer as a whole but on single chips. 200 nm 'CuPc' is deposited on the first sample and 100 nm on the second sample. The reason behind taking two different deposition profiles is,

(i) as it was hard to perform electrical measurements on the first sample, a lesser amount was deposited for the second sample.
(ii) the organic channel thickness should influence the electrical transport, the spin transport phenomena and at the end the magnetoresistance.

As the minimum trench width is 100 nm, it is wise to deposit 'CuPc' in 100-200 nm range. The next step would be to have images of the structures. The samples are cut to reach proper

structures not manually but by FIB method. FIB technology somewhat resembles SEM method where SEM uses focused beam of electrons (for imaging) and FIB uses focused beam of ions (direct stream of positively charged massive ions are heavier and larger than the electrons and thus can sputter or expel away the materials from the surface very easily). Gallium ions can be used. FIB finds interest on semiconductor technology, material science and natural science domains but care should be taken such that this technology does not damage much of the wafer or sample portion. FIB is now a days used to make probe holes, cutting a sample to investigate further or even in failure analysis or repair [34]. After cutting the samples with FIB, the SEM images are taken by providing a protective layer onto the samples.
One thing is noted down. The samples are prepared from the wafers by 'dicing', using a UV light transparency to protect them during the process.

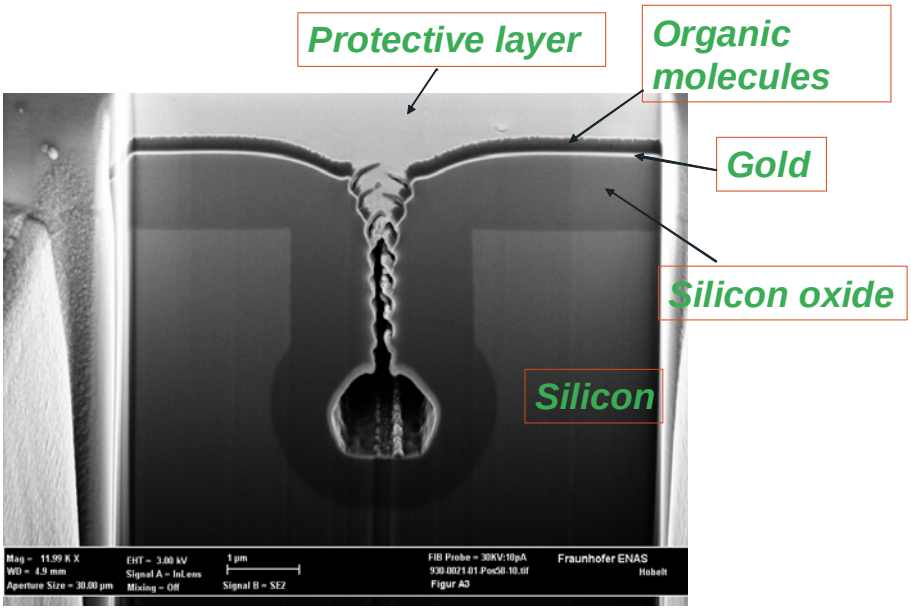


Figure 5.21: This image shows the first sample (i.e. 200 nm 'CuPc'). Every part of the image is depicted. It is noted that the image does not reveal that much whether the organic molecules can fill up the trenches fully but it seems that they can fill up a portion. No organic channel is noted to be formed exactly at the surface of the trench. This structure is 'A3' and hence the lowest width one. The growth mode seems to be layer by layer.

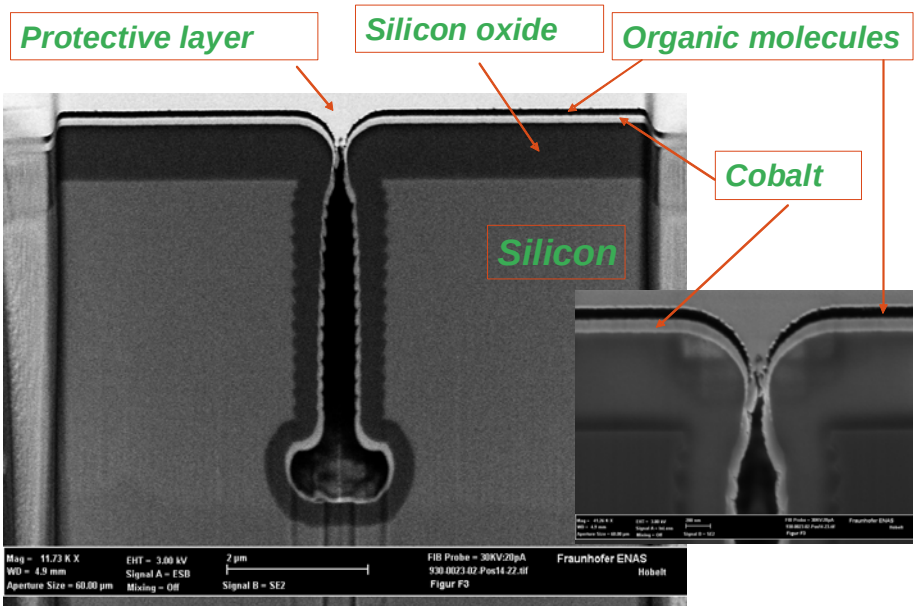


Figure 5.22: These two images show the second sample (i.e. 100 nm 'CuPc'). Every part of the image is depicted. This structure is 'F3'. It is noted that the organic molecules do not seem to be filling up the trenches properly, the formed channel seem to be discontinuous near the trench. Again, the films show non conformal behaviour, they get thinner inside the trenches compared to the top surface.

6. Discussion and summary

This part depicts the different targets achieved so far and all kinds of future modification and scope for further working as well.

In this project, there were some challenges regarding the device fabrication as mentioned before in the 'Introduction' part and in the subsequent parts. The first challenge has been to check how one can achieve trenches less than 200 nm perfectly (without using nanolithographic process) and then to check whether one can fill up those trenches properly by chemicals. Both TO and LPCVD methods to shorten the trench width worked and LPCVD profile was preferred. In both of the cases, it never happened that only the surface is open but trenches are fully covered by oxide (even in the 100 nm range) which is a good thing. If that was the case, a further metal deposition step would have short circuited the structures very easily. Another interesting thing was when the metal was deposited; one could avoid any kind of short circuit (even when the trench opening was around 100 nm) which is also a good thing. The concept of isotropic etching (of the bottom Si surface) to avoid metal short circuit worked and by the help of sputtering, the metal gets deposited only in the side walls, the probability of the metal to make a continuous layer at the surface or even inside the trenches is much less. These are excellent findings from technology perspective and these steps prove that it is possible to cope up to the downscaling concept and the device can be used for further spintronics investigation.

The first step was to fill up with photoresist materials (this was successful) but the trenches were somewhat of higher width. Both spin and spray coating methods were successful; at least they could fill up 400 nm width and more than 3 um depth trenches (as far as the SEM images reveal). The second step was to fill up by the original organic molecules. How the trenches would transport charge, how organic channels are formed etc everything depends on the filling technique. The proper attempt was taken to cut the samples accurately near the trenches and check for the organic layers. It is noticed that the images are not very clear or one can not predict exactly how the channels are formed. The electrical testing gave good results which means the organic layer might not be discontinuous near the trenches (they can carry electrons). If they were discontinuous, one could have got open circuit which is not the case. It is also mentioned here that a FIB could highly damage the organic layers so that the SEM images might well be somehow misleading.

<u>Scope of further work:</u>

(1) First attempt should be taken to try for low ion energy FIB to avoid any kind of (a) organic layer damage (b) protective layer damage (c) intermixing between these two layers. This would be followed by SEM images.
(2) It is important to ensure that the charge transport happens only through the desired trenches (not any of the isolating ones). So, some more samples should be prepared for electrical testing as it was possible only for a single sample. One can think about a control on the deposition rate as well.
(3) Electrical measurements are the first set of experiments. Voltage should be varied carefully with a certain time constant and low voltage range should also be studied (say, 0 to 1 V in steps of 0,1 V). As scratching of the molecules is a problem (to reach

the metallic part for outer connection), one can think about selective deposition process of the organic molecules (use of further masking).

(4) Vary the metal thickness (say, 50 nm, 75 nm, 100 nm instead of only 100 nm) and prepare more samples. This dimension can influence ferromagnetic properties of 'Co'.

(5) The one of the major steps is obviously study magnetoresistance i.e. vary the magnetic field, change magnetization in the ferromagnets and study the change in electrical resistance. As the structures have varying transport dimensions, current vs channel length under constant magnetic field could also be noticed. For a transport length >300 nm, the current should be almost vanished.

(6) Current as a function of temperature could also be studied as ferromagnetism property is highly affected by temperature influence.

(7) If the downscaling concept works after finishing all these experiments, one can think about depositing other molecules and investigate for spintronics device further.

Appendix A:

Wafer grid image is shown; this is typically a top view of all the wafers.

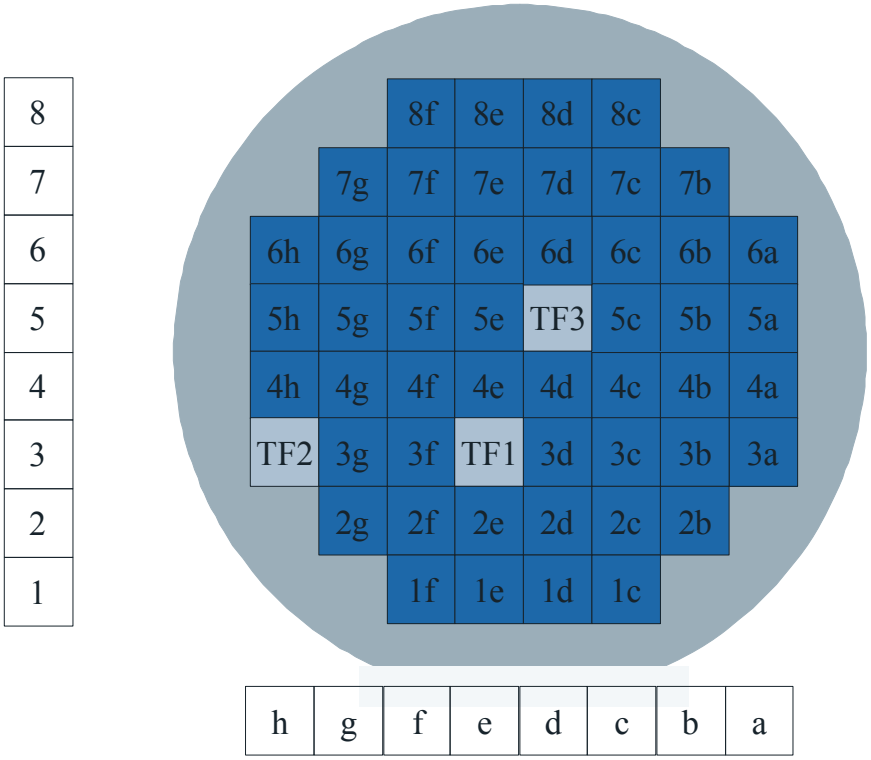


Figure (a): This picture shows the wafer grid image with proper numbering

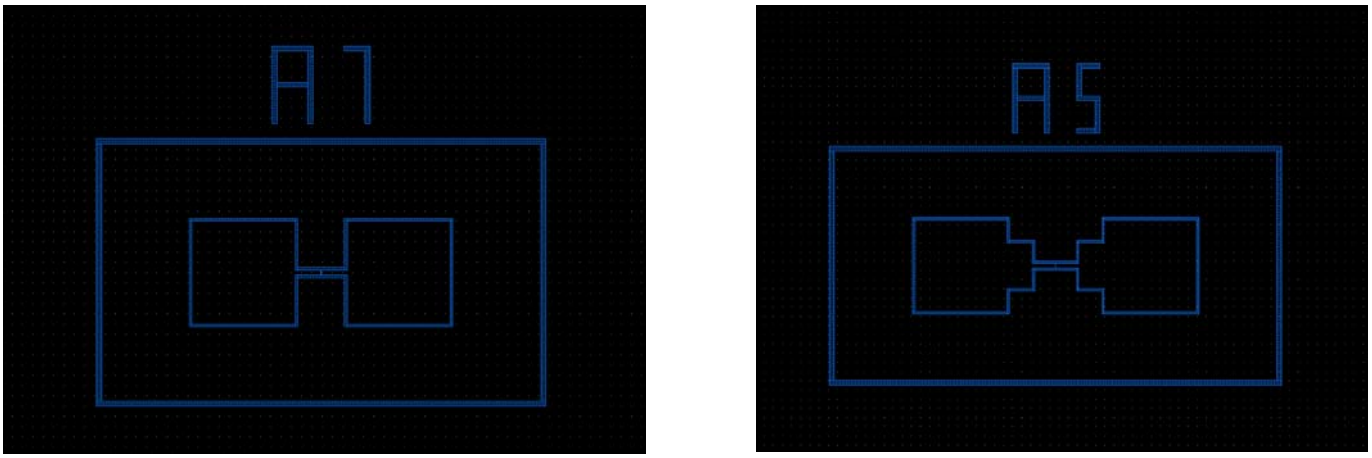


Figure (b1): Layout showing the basic units used

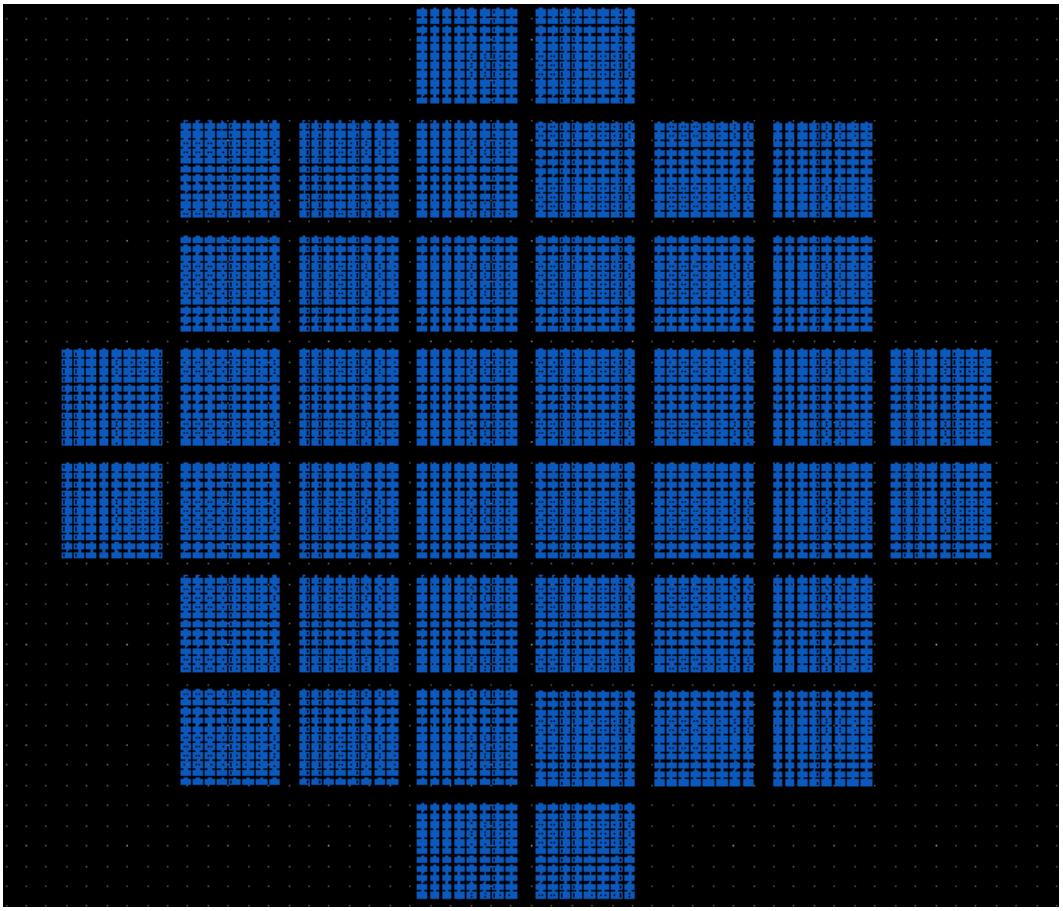


Figure (b2): Layout developed for the wafer

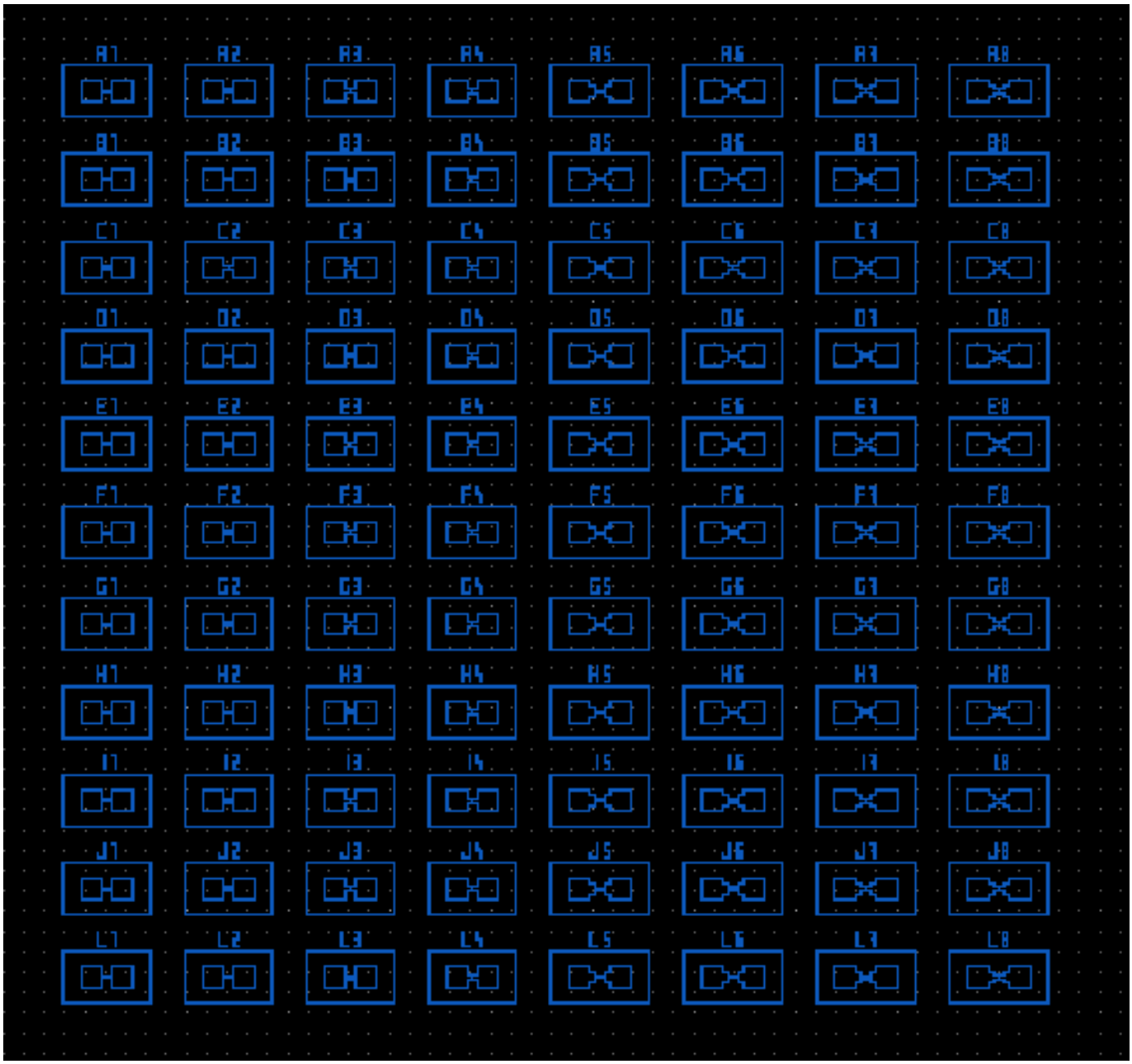


Figure (b3): Picture showing layout editor design of the structure, all the different types of geometries are present.

Appendix B

Properties of Copper Phthalocyanine:

(a) Electrical susceptibility is anisotropic, it ranges from 2,3 to 4,1 when analyzed in DC domain.
(b) Magnetic susceptibility typically ranges in between 10^{-4} to 10^{-6}.
(c) Electric resistance should vary from Mega to Giga Ohm.
(d) Available in blue, odourless, powdered form.
(e) This melts at above 250 °C.
(f) 'CuPc' is thermally stable compared to other complexes.
(g) Energy band gap (electronic) is less than 2 eV, 'CuPc' being an organic semiconductor.
(h) In organic electronics group, Fullerene (C_{60}) and 'arylene diimide' family could be operated as 'n' type semiconductors and Phthalocyanine groups, pentacene etc. are used as 'p' type ones [35] [36].

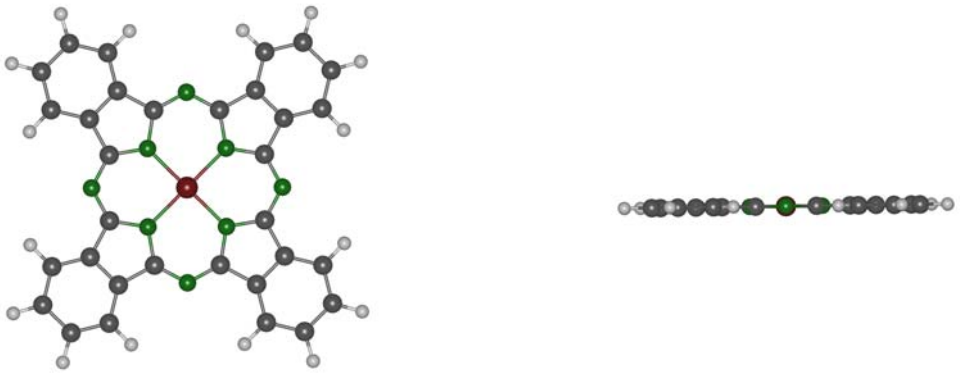
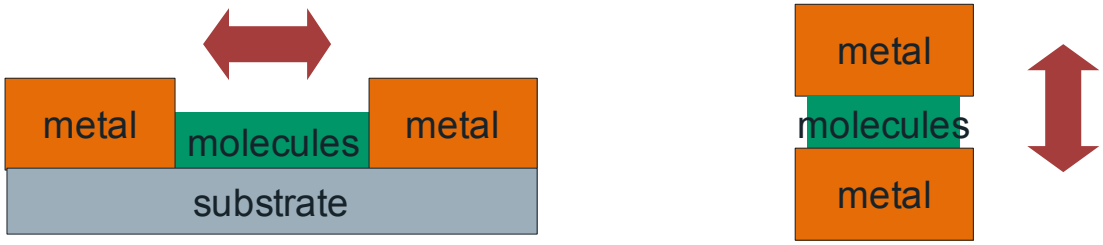


Figure (c): (Cu) Phthalocyanine group ($C_{32}H_{16}CuN_8$). The first picture shows the front view of the molecule (red molecule is Copper, green ones are Nitrogen, gray one are Carbon and the light gray coloured molecules are Hydrogen). The second picture shows the side view (the molecule is coplanar).

Appendix C

Molecular transport:



Lateral transport

Vertical transport

Figure (d): These pictures show the transport channel being sandwiched between two electrodes. Charge transport is realized in above mentioned two ways. The second one can be realized by 'rolling up' nanotechnology.

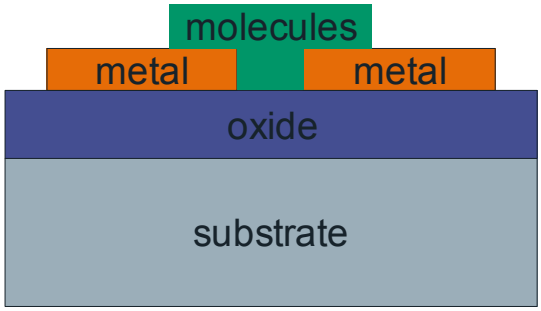


Figure (e): This picture shows one of the possibilities of a laterally stacked device, but being fabricated by nanolithography. The process steps would be different. In this technology, one needs to etch away only the metal part (around 200 nm, the metal resting on an oxide film) rather than the oxide.

Appendix D

List of tables:

Appendix E

List of pictures:

Appendix F:

Literature study:

[1] Shaw, K. A.; Zhang, Z. L.; MacDonald, N. C.: "SCREAM I: a single mask, single-crystal silicon, reactive ion etching process for microelectromechanical structures", Sensors and Actuators A v. A40, no. 1, Jan. 1994, pp 63-70.

[2] Fedder, G. K.; Santhanam, S.; Reed, M. L.; Eagle, S. C.; Guillou, D. F.; Lu, M. S.; Carley, L. R.: "Laminated high-aspect-ratio structures in a conventional CMOS process", Sensors & Actuators A, v. 57, no. 2, 1997, pp 103-110.

[3] Parameswaran, M.; Baltes, H. P.; Ristic, L.; Dhaded, A. C.; Robinson, A. M.: "A new approach for the fabrication of micromechanical structures ", Sensors and Actuators, v. 19, no. 3, 1989, pp. 289-307.

[4] Zhang, Z. L.; MacDonald, N. C.: "A RIE process for submicron silicon electromechanical structures", J Micromech Microeng, 2 (1992) pp.31-38.

[5] Binasch, G.; Gruenberg, P.; Saurenbach, F.; Zinn, W.; Phys. Rev. B39, 4828 (1989).

[6] Wolf, S. A.; et al., Science 294, 1488 (2001).

[7] http://www.freepatentsonline.com/y2010/0006840.html USA patent US20100006840.

[8] Korvink, Jan. G.; Paul, Oliver: "MEMS, a practical guide to design, analysis, and applications", William Andrew publishing, 2006.

[9] Cao, Guozhong: "Nano structures and nano materials, synthesis, properties and applications", Imperial college press, 2005.

[10] Smith, Donald: "Thin film deposition, principles and practice", McGraw-Hill, Inc, International edition, 1995.

[11] Brosnihan, T. J; Bustillo, J M; Pisano. A. P. and Howe, R.T.; "Embedded interconnect and electrical isolation for high-aspect-ratio", Transducers 97, Chicago, USA, pp 637–640, 1997.

[12] Wei, J.; van der Velden, M.; Sarro, P. M.: "Fabrication of vertical electrodes on channel sidewall for picoliter liquid measurement", Transducer 2007, Lyon, France, Jun, 2007.

[13] Verma, H. C.: 'Concepts of physics', Bharti bhawan (publishers and distributors), 1999 reprint.

[14] Barry Carter, C.; Grant Norton, M.: "Ceramic materials: science and engineering", Springer, April 2007.

[15] Zutic, I.; Fabian, J. and Das Sarma, S.: “Spintronics: Fundamentals and applications”, Rev. Mod. Phys. 76, 323 (2004).
[16] Biedenharn, L.C. and Louck, J.D.: “Angular Momentum in Quantum Mechanics”, vol. 8 of the Encyclopedia of Mathematics (AddisonWesley, 1981).

[17] Brodie, Ivor and Muray, J.J.: “The Physics of Micro/Nano-Fabrication (Microdevices)”, Academic press, 2007.

[18] Middleman, S.; Hochberg, A.K.: “Process Engineering Analysis in Semiconductor Device Fabrication“, McGraw-Hill, 1993.

[19] Dyakonov, M. I.; Perel, V.I.: “Possibility of orienting electron spins with current”, JETP Lett. 13, 467 (1971).

[20] Hirsch, J. E. “Spin Hall effect“, Phys. Rev. Lett. 83, 1834 (1999).

[21] Zhang, S.: “Spin Hall effect in the presence of Spin diffusion“, Phys. Rev. Lett. 85, 393 (2000).

[22] Grünberg, P.; Schreiber, R.; Young, Y.; Brodsky, M., B.; Sowers, H. Phys. Rev. Lett. 57 (1986) 2442.

[23] Baibich, M.N.; Broto, J., M.; Fert, A.; Nguyen Van Dau, F.; Petroff, F.; Etienne, P.; Creuzet, G.; Friederich, A.; Chazelas, J. Phys. Rev. Lett. 61 (1988) 2472.

[24] Datta, S.; Das, B. Appl. Phys. Lett. 56 (1990) 665.

[25]. Ohno, H., et al., Appl. Phys. Lett. 69 (1996) 363.

[26] Kato, Y.; Myers, R., C.; Gossard, A., C.; Awschalom, D., D. Science 306 (2004) 1910.

[27] Bhardwaj, J., K.; Ashraf, H.: “Advanced Silicon Etching Using High Density Plasmas”, Proc. SPIE Micromachining and Microfabrication Process Technology, Vol. 2639, pp.224-233, (1995).

[28] Bhardwaj, J., K.; Ashraf, H.; McQuarrie, A.: “DRY SILICON ETCHING FOR MEMS”, Prince of Wales Industrial Estate Abercarn, Gwent, NP1 5AR, UK.

[29] O’Handley, Robert: “Modern Magnetic Materials, Principles and Applications”, John Wiley & sons, Inc., 2000.

[30] Prince, Betty: “Semiconductor memories: A Handbook of Design, Manufacture and Application”, John Wiley & sons, Inc., second edition, Feb 1995.

[31] Gerlach, G.; Dötzel: “Introduction to Microsystem Technology, A guide for students”, John Wiley & sons, Inc., second edition, Feb 1995.

[32] Dediu, V.; Murgia, M.; Matacotta, F., C.; Taliani, C.; Barbanera, S.: “Room temperature spin polarized injection in organic semiconductor”, Solid State Communications 122 (2002), pp 181-184.

[33] Coey, J., M., D.: “Magnetism and magnetic materials”, Cambridge university press, 2010.

[34] Yao, Nan: “Focused Ion Beam System: Basics and Applications”, Cambridge university press 2007.

[35] Jones, William: “Organic Molecular Solids: Properties and Applications”, CRC Press, ISBN: 0-8493-9428-7

[36] Y., Yu, Peter; Cardona, Manuel: “Fundamentals of Semiconductors, physics and material properties”, Springer 2005, 3rd edition.

[37] Jaeger, Richard C.: "Thermal Oxidation of Silicon, Introduction to Microelectronic Fabrication”. Upper Saddle River: Prentice Hall, 2002.

Appendix G:

Acknowledgement:

I would like to thank,

- to my Prof. Thomas Gessner for giving me the opportunity to work in the Microtechnology department. I came here in this university in Germany for working in Nanotechnology field.
- my two supervisors, Dr. Danny Reuter and Dr. K. Hiller for all their support and suggestions with proper guidance towards the project, at the initial stage and also during the processes.
- to Prof. Salvan and Prof. Zahn from 'Physik' department for their help in understanding the total project of 'Towards Molecular Spintronics', TMS.
- Dr. Bertz, Ms. Bruder, Mr. Klimmt, Mr. Küchler, Mr. Werner from 'Lithography' department for helping me to develop the structures.
- Mr. Zichner, Miss Kowol, Mr. Plänitz from 'Layer Deposition' department.
- Dr. Schulze and Mr. Ludwig from 'Physik' department for helping us taking good quality SEM images.
- Dr. Michael Fronk from TMS project for giving suggestions.
- Dr. Jürgen Bräuer from 'Elektrotechnik und Informationstechnik' department for assisting me about different course works and research opportunities in this university.
- my classmates and junior friends, also my other friends who are studying here.
- last but not least, I thank all my family members, my parents, my sister for their eternal love and constant support. Thanks to all joy and pain, happiness and sorrow, opportunities and difficulties which I faced in these years. They are the finest memories in life to treasure.

Statutory declaration statement:

I hereby affirm that I have written all the notes by use of a series of literature study. I, with the useful help of my supervisors, colleagues and necessary usage of software, have done all these works on my own.

Joydeep Ghosh